Fast Hierarchical NPN Classification

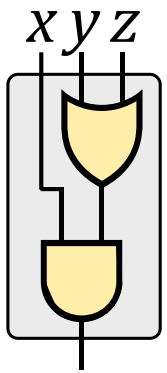
Ana Petkovska, Mathias Soeken, Giovanni De Micheli,
Paolo Ienne, and Alan Mishchenko

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Berkeley
UNIVERSITY OF CALIFORNIA

August 30, 2016
Lausanne, Switzerland

Negation-Permutation-Negation (NPN) Classification



$f(x, y, z) = x(y + z)$

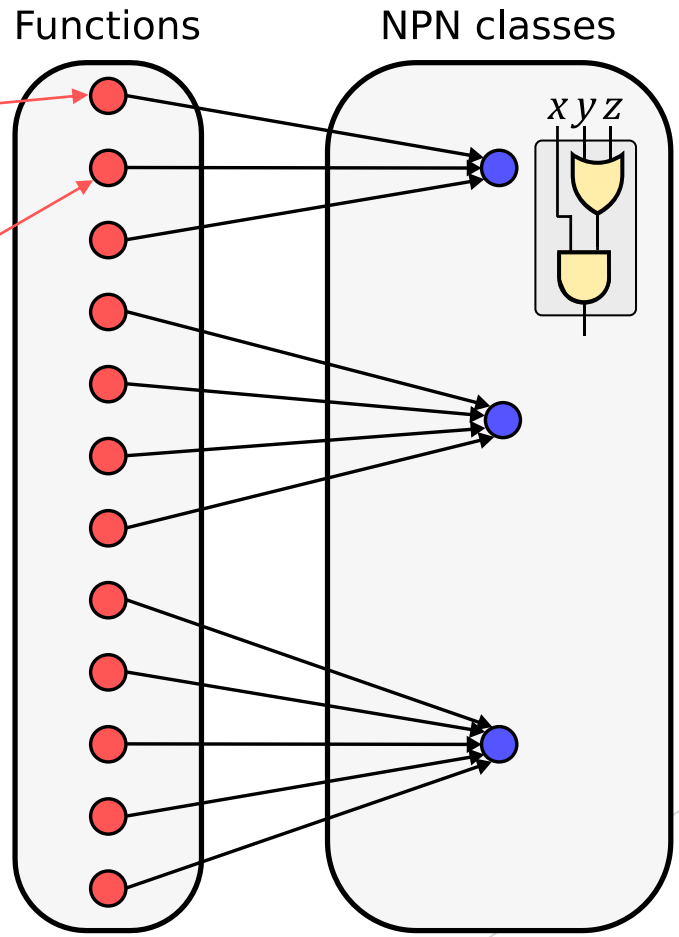
NPN equivalent
permute x and y
negate x

$g_1(x, y, z) = y(\bar{x} + z)$

$g_2(x, y, z) = x(z + y)$

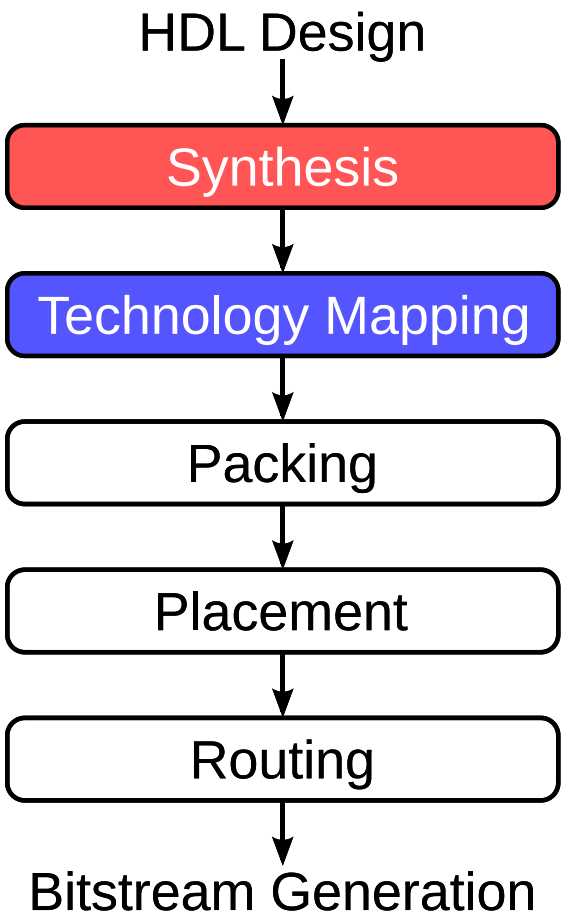
$g_3(x, y, z) = \bar{x} + \bar{y}\bar{z}$

$g_4(x, y, z) = \bar{y} + xz$



functions > # NPN classes

NPN Classification: Part of the FPGA Design Flow

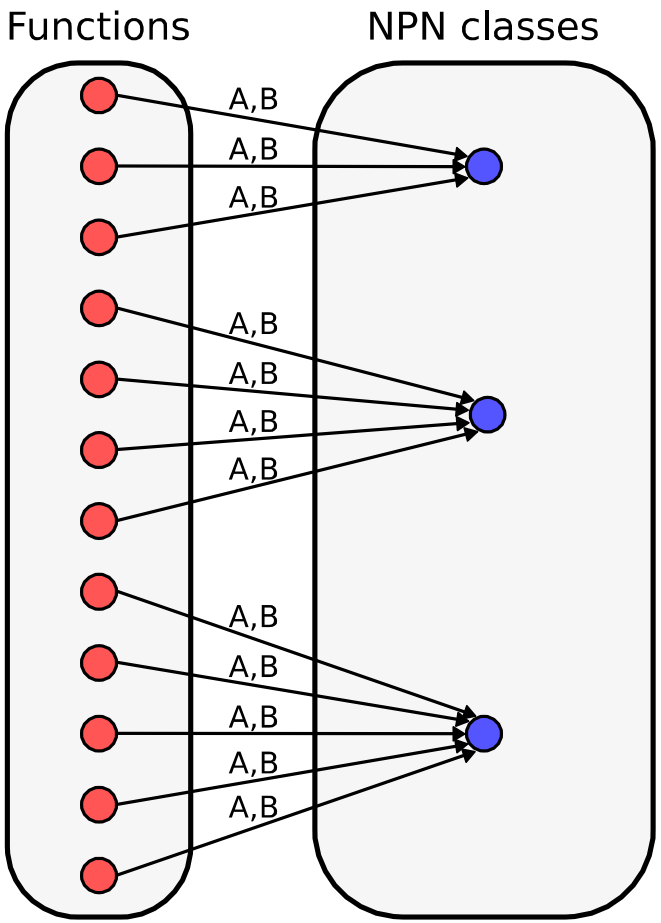


- For building compact libraries of circuit structures or cuts produced by different tools and benchmarks.
- For retrieving an optimal structure for a given Boolean function from a library.
- For matching Boolean functions of millions of enumerated structural cuts against a library of cells used to implement the design.

- W. Yang et al., “Lazy man’s logic synthesis”, ICCAD’12
- A. Kennings et al., “Efficient FPGA resynthesis using precomputed LUT structures”, FPL’10

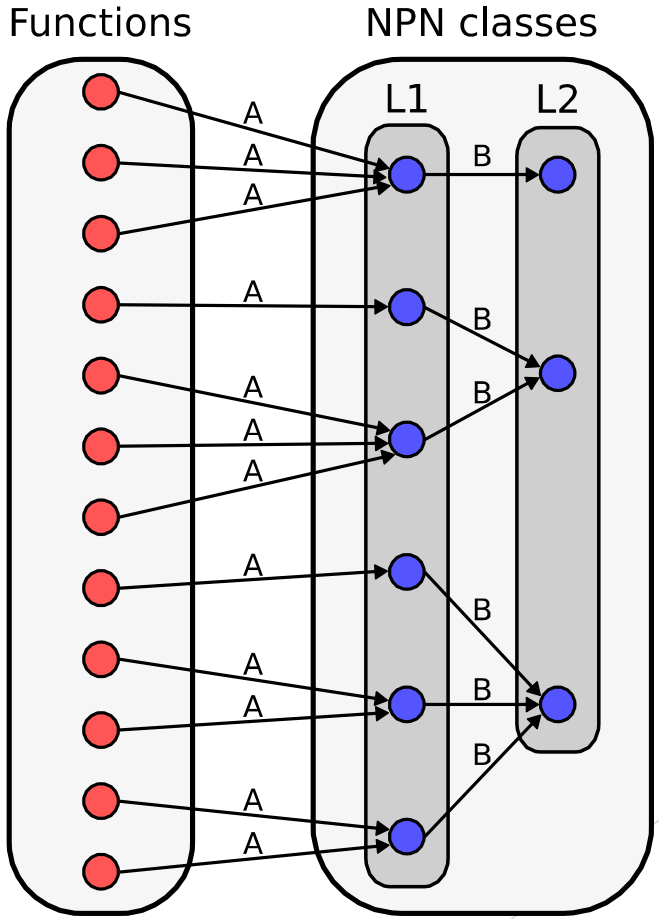
- A. Mishchenko et al., “Combinational and sequential mapping with priority cuts”, ICCAD’07
- A. Mishchenko et al., “Technology mapping into general programmable cells”, FPGA’15

Algorithms for NPN Classification



Existing algorithms

Discard intermediate results



Our algorithm

Keep intermediate results as a hierarchy of classes

Experimental Results: Runtime Comparison

- Classification of full-DSD functions

#Inputs	#Func	State-of-the-art Heuristic	Hierarchical Approach (Heuristic)	Exhaustive Exact Algorithm	Hierarchical Approach (Exact)
6	1M	0.28 s	0.10 s	33 min	0.20 s
8	1M	0.80 s	0.22 s	> 12 h	59.34 s
10	100K	0.19 s	0.09 s	> 12 h	2.56 h

3.7x faster
max. 160 MB more memory

exact classification
for small functions
in seconds