# An Evaluation on the Accuracy of the Minimum Width Transistor Area Models in Ranking the Layout Area of FPGA Architectures
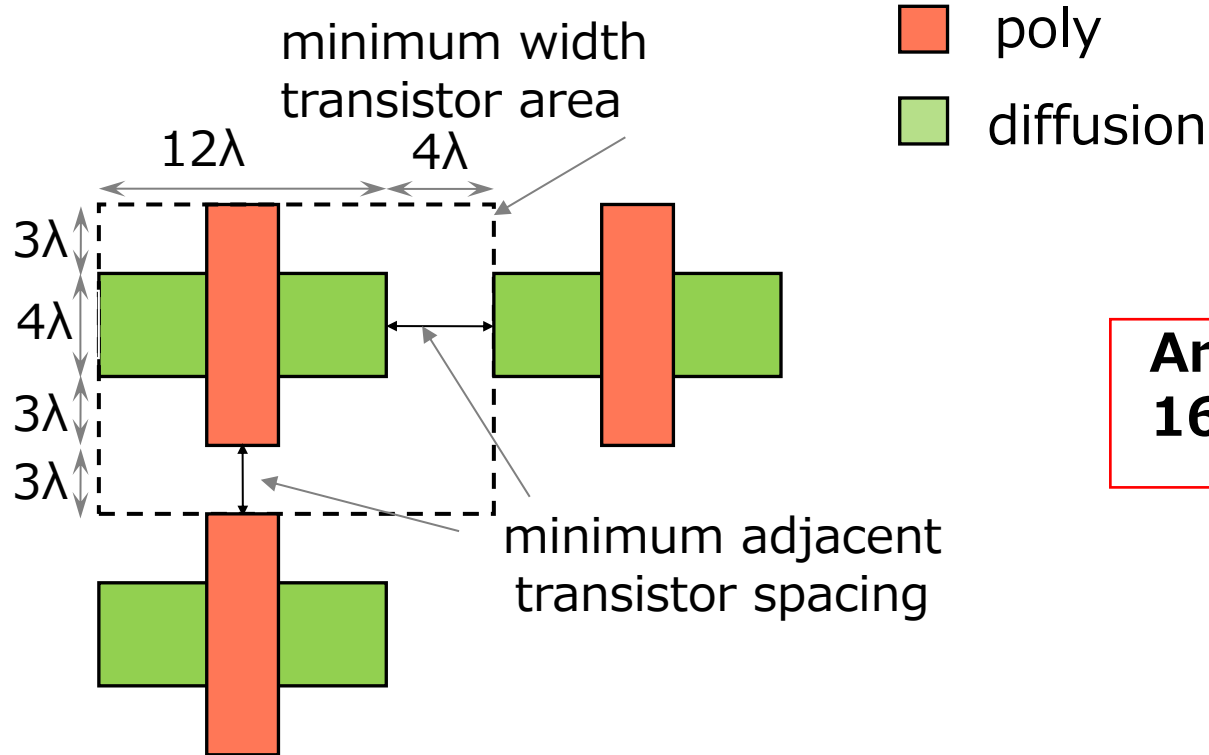
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Ryerson University, Canada

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# Motivation

➤ Increasing FPGA based SOC designs

➤ Reconfigurable fabrics benefit applications

➤ Non-FPGA companies may use FPGA fabric

➤ Accurate estimation of layout area

➤ Early floorplanning

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# Current Area Model

poly

diffusion

minimum width
transistor area

12λ        4λ

3λ

4λ

3λ

3λ

**Area in terms of λ**
**16λ x 13λ= 208λ²**

minimum adjacent
transistor spacing

**Drawback –** wiring & diffusion sharing not considered

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# VPR Area Model

➤ **Area(x) =** $0.5 + 0.5x$

$$\boxed{\textbf{1 mwt = 208}\lambda^2}$$

• **Area in terms of λ**

        **when** $x=1$ ; **1 mwt -> 208$\lambda^2$**

                    $x=2$ ;**1.5 mwt -> 312$\lambda^2$**

# COFFE Area Model

$$1 \text{ mwt} = 208\lambda^2$$

➤ **nMOS transistors**
- **Area(x) =** $0.447 + 0.128x + 0.391\sqrt{x}$

    when x=1 ; **0.97 mwt -> 200.93λ²**

➤ **CMOS transistors**
- **Area(x) =** $0.518 + 0.127x + 0.428\sqrt{x}$

    when x=1 ; **1.07 mwt -> 223.18λ²**

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# FPGA building blocks

➢nMOS based Components

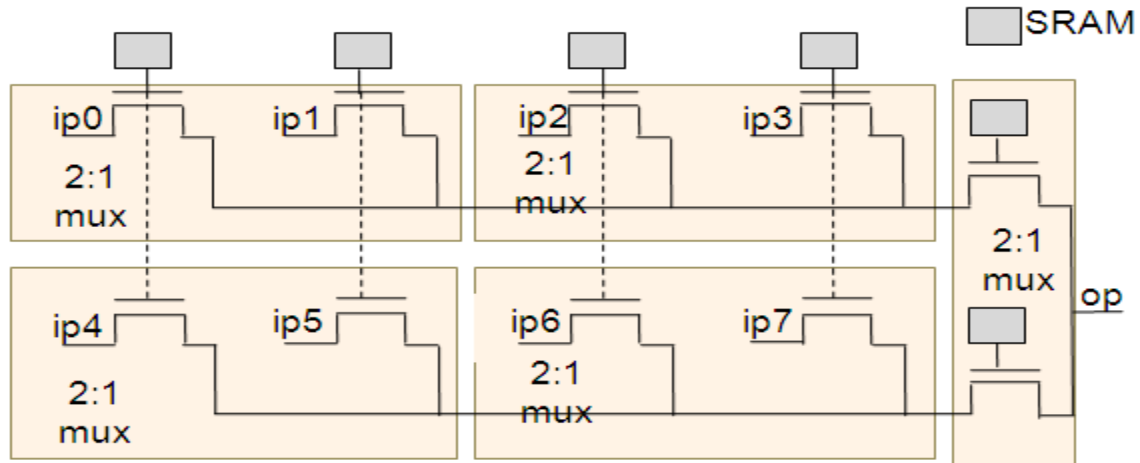• Encoded and Decoded Multiplexers

➢CMOS based Components

• Buffers

• Full adders

**Models accuracy at ranking different FPGA architectures ?**

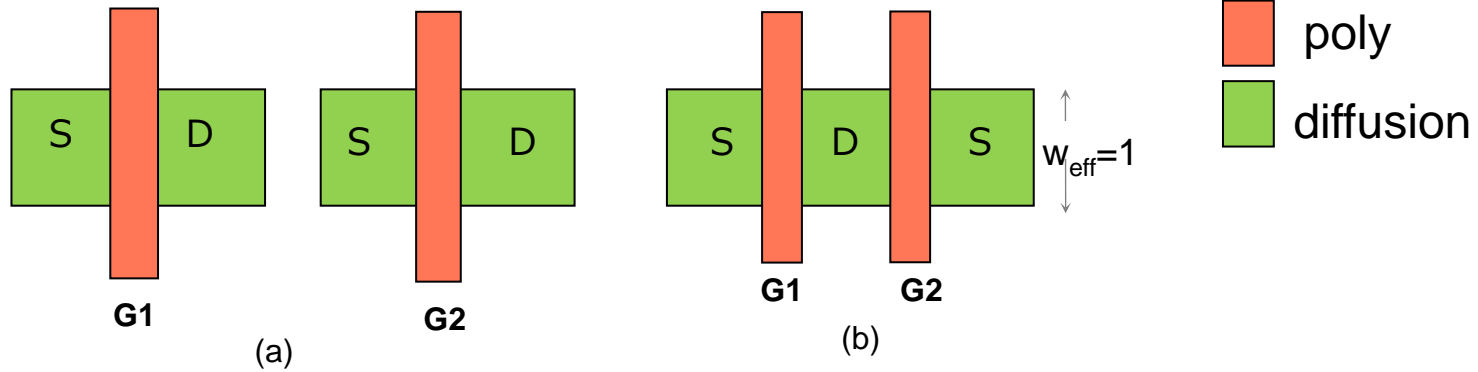# Encoded Multiplexer
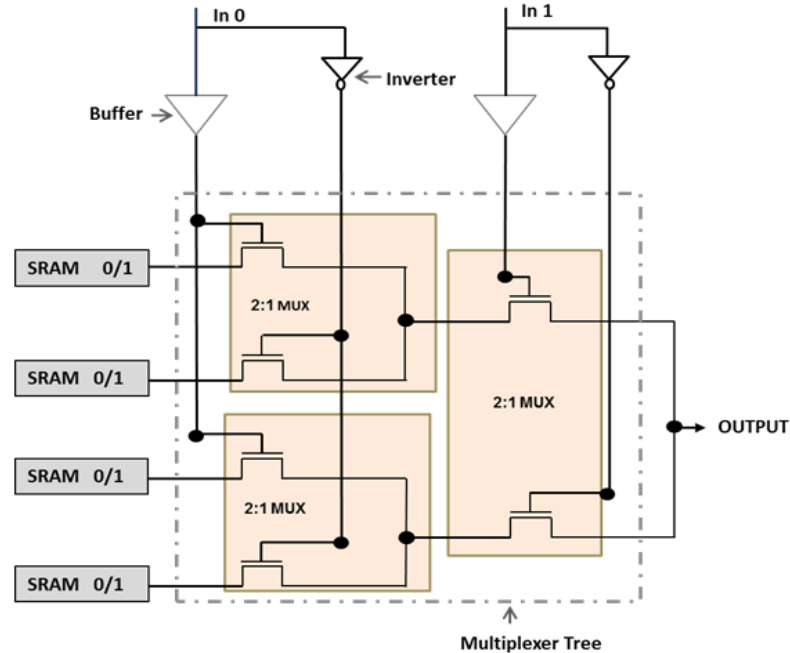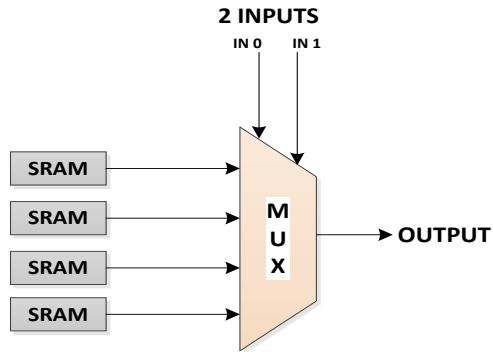


- 2:1 LUT

- 4:1 Encoded Multiplexer

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# Decoded Multiplexer



- 8:1 Decoded Multiplexer

- two level multiplexer

# 2:1 Multiplexer



S D   S D
G1   G2
(a)

S D S   $w_{eff}=1$
G1   G2
(b)

poly
diffusion

Two discrete transistors

Transistors with diffusion sharing

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# Effect of folding on area
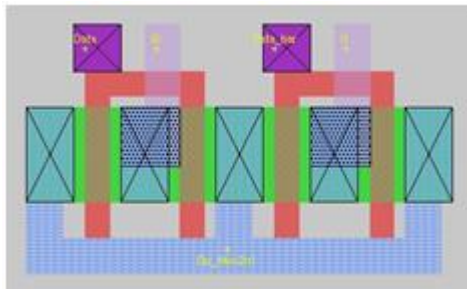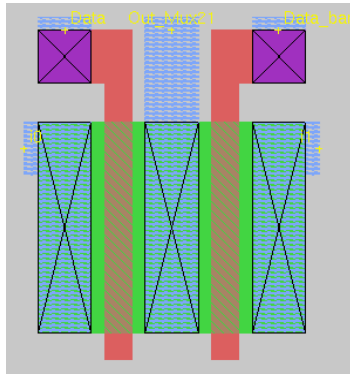


| Transistor size | without folding | with 2 folds | with 3 folds |
|---|---|---|---|
| 4x | $600\lambda^2$ | $680\lambda^2$ | $802\ \lambda^2$ |
| 6x | $792\lambda^2$ | $840\lambda^2$ | $952\lambda^2$ |
| 10x | $1176\lambda^2$ | $1160\lambda^2$ | $1250\lambda^2$ |
| 12x | $1368\lambda^2$ | $1320\lambda^2$ | $1400\lambda^2$ |

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# Transistors with small drive strengths



minimum width transistor area

poly

diffusion

$5*4\lambda$        $4\lambda$

$3\lambda$

$w_{eff}(4\lambda)$

$3\lambda$

$3\lambda$    $4\lambda$    $1\lambda + 2\lambda + 1\lambda$

minimum adjacent transistor spacing
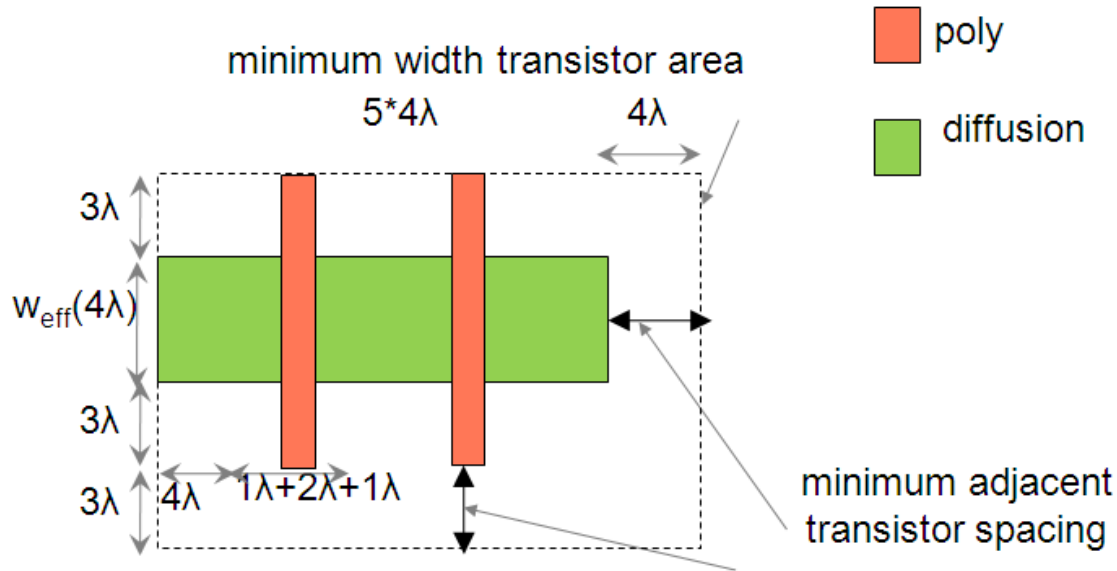
$$Active\_Area_{2:1mux} = (9 + 4w_{eff})24\,\lambda^2$$

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# Transistors with large drive strengths



minimum width transistor area

$(4n+1)4\lambda$    $4\lambda$

poly

diffusion

$3\lambda$

$\dfrac{w_{eff}(4\lambda)}{n}$

$3\lambda$

$3\lambda$

minimum adjacent transistor spacing

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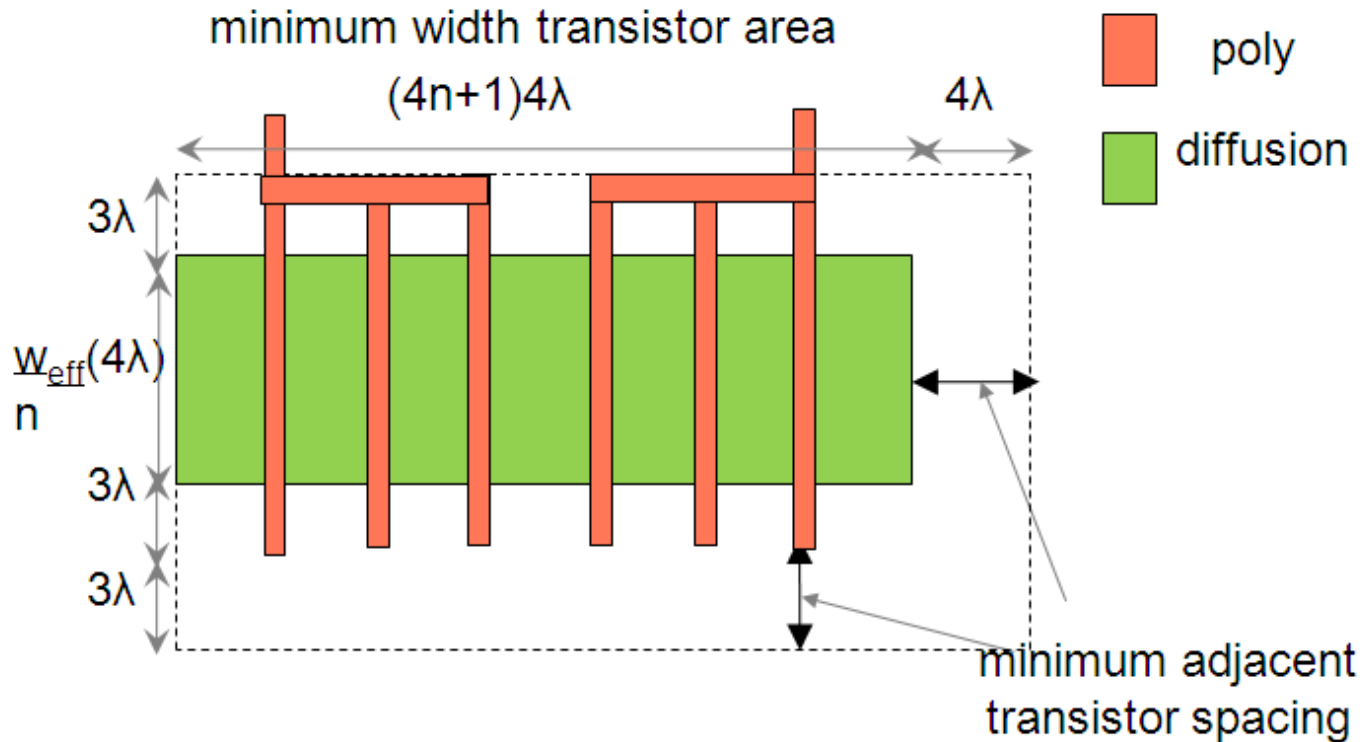
$$Active\_Area_{2:1mux} = \frac{(9n + 4w_{eff})(2n+1)8}{n}\lambda^2$$

**Differentiating with respect to n**

$$\frac{\partial Active\_Area_{2:1mux}}{\partial n} = \left( \frac{18}{26} - \frac{4w_{eff}n^{-2}}{26} \right)mwt = 0$$
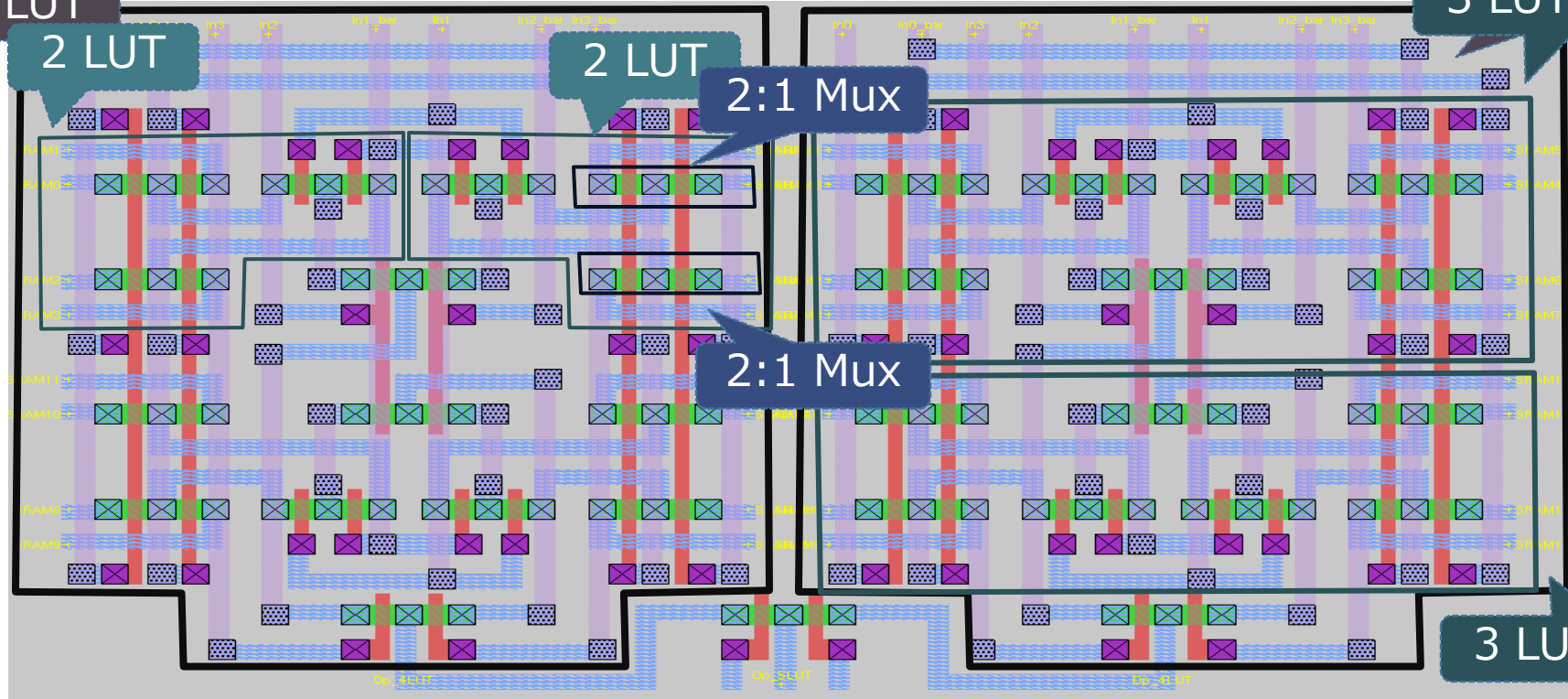
**Note, if n=1, the above equation is the same as previous equation**

$$n^2 = \frac{4w_{eff}}{18}$$

$$Active\_Area_{2:1mux} = \frac{(9n + 4w_{eff})(2n+1)8\lambda^2}{n \times 208\lambda^2} \ mwt$$

$$n = \left[ \frac{\sqrt{2w_{eff}}}{3} \right] = \left[ 0.471\sqrt{w_{eff}} \right], n \geq 1$$

$$= \frac{(9n + 4w_{eff})(2n+1)}{26n} mwt$$

$$n \ is \ the \ number \ of \ folds \ of \ transistor$$

$$with \ drive \ strength \ w_{eff}$$

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# Layout Strategy

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# Mirroring Technique  5 LUT
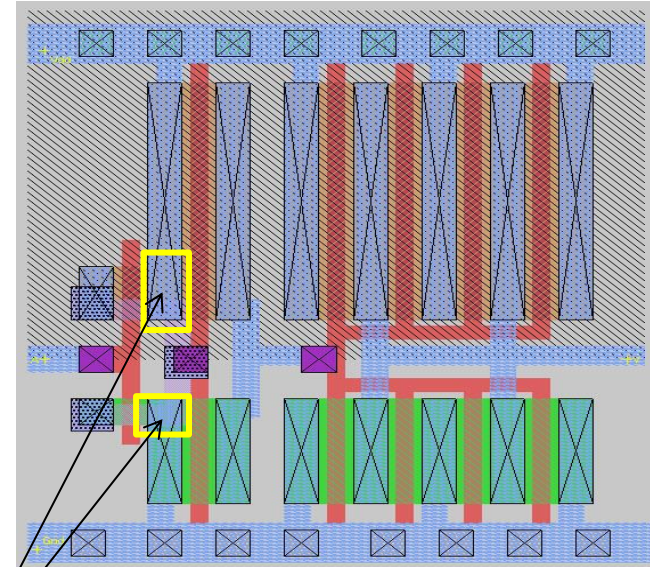
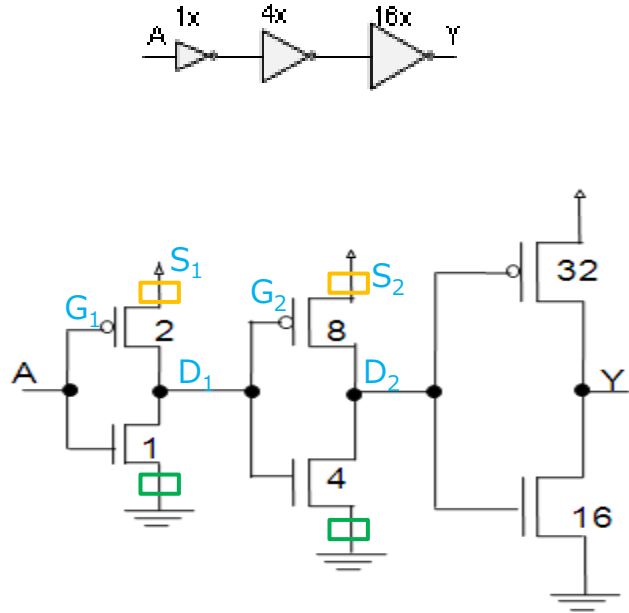Everyone Makes a Mark

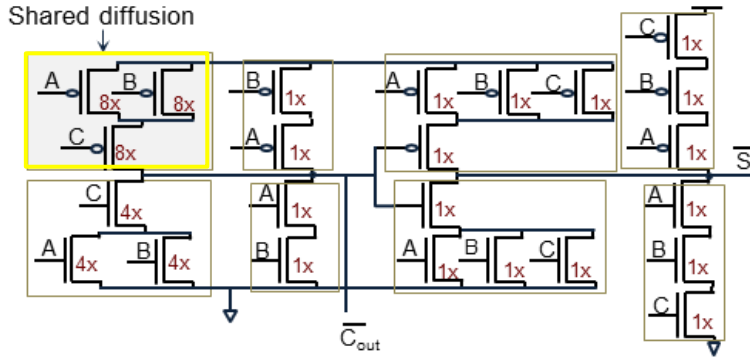# Layout strategy for decoded multiplexer
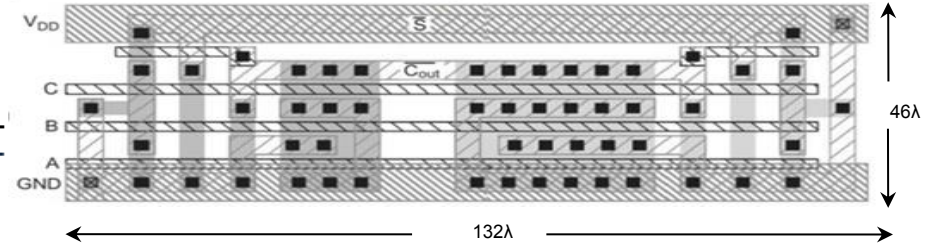
2:1 mux
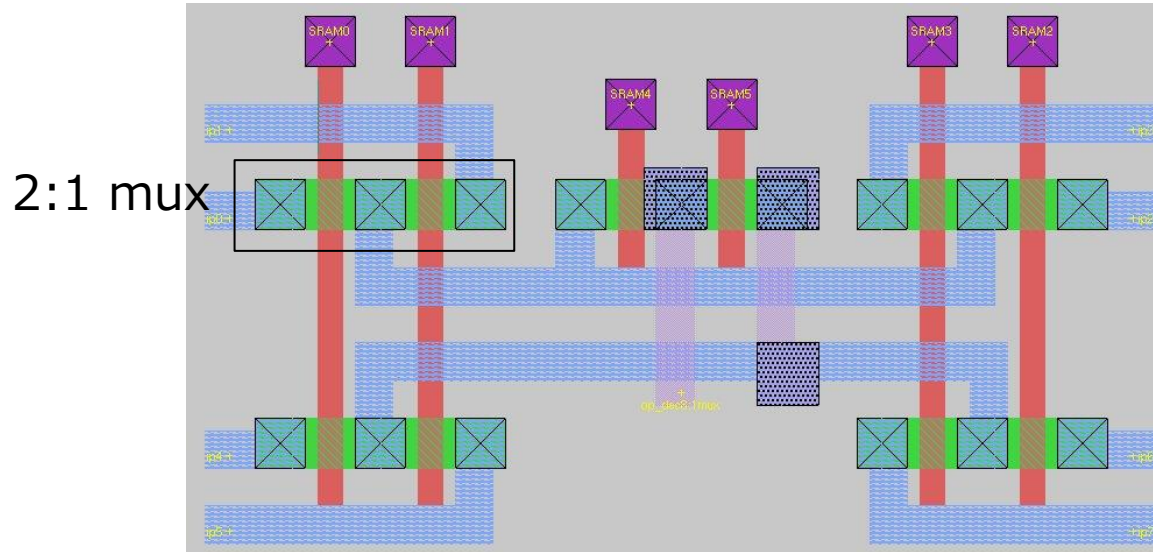
# Buffers - Multistage Buffer



**diffusion sharing**

# Full adder



schematic



layout

# Results

➢**Active area comparison**

➢**Layout area**

- number of metals used

- **Encoded & Decoded multiplexer**

  .1x transistor size

  .change in transistor size

- **CMOS based components**

  .buffers and full adder

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# Active area calculation

➢ **Encoded Multiplexer**
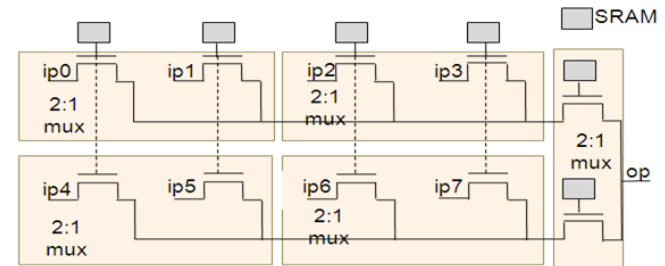
$$Active\_Area_{k-LUT} = (2^k - 1)Active\_Area_{2:1mux}$$

**k is number of inputs to LUT**
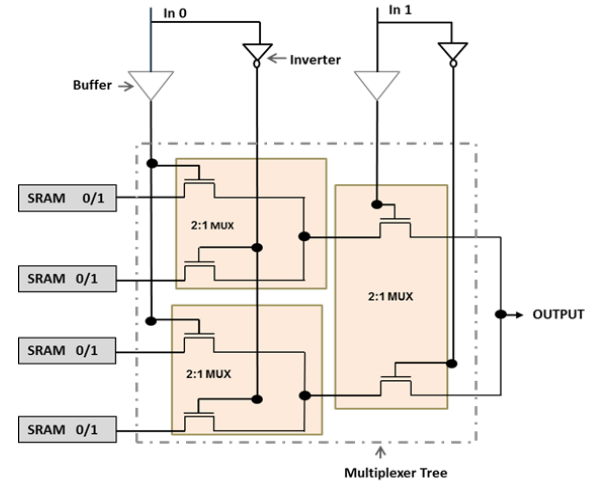
➢ **Decoded Multiplexer**

$$Active\_Area_{z:1\ dmux} = (\frac{z}{2} + 1)Active\_Area_{2:1mux}$$

**z is number of inputs to decoded multiplexer**

# Active area comparison – Part I

**Active Area - Encoded and Decoded Multiplexers**

**Difference**

Legend: ■ VPR  ■ COFFE

Y-axis: 160%, 140%, 120%, 100%, 80%, 60%, 40%, 20%, 0%, -20%

X-axis (Transistor size): 1 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34
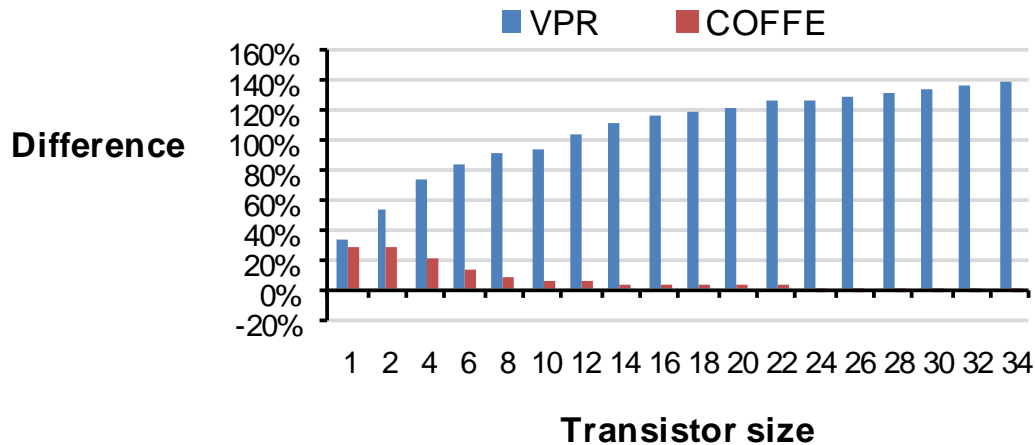
**Transistor size**

**VPR : overestimates**
33% to 139%

**COFFE** : - **overestimates**
for 1x - 6x transistor sizes 14% to 29%
        - very close for large transistor sizes

# Part II



**Active Area - CMOS components**
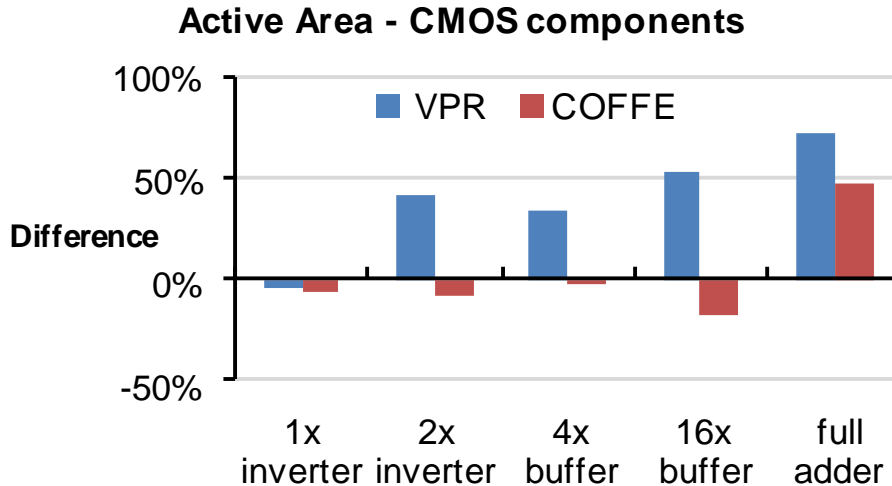
**VPR :** - **underestimates** 1x inverter **4%**
- **overestimates** larger inverters, buffers & full adder **72%**

**COFFE** : - **underestimates** for inverters **18%**
- **overestimates** for full adder **46%**

# Full layout area metal layers

## Example : INTEL 45nm Metal Stack

| Layer | thickness(nm) | width(nm) | pitch(nm) |
|:---:|:---:|:---:|:---:|
| M9 | 7 µm | 17.5 µm | 30.5 µm |
| M8 | 720 | 400 | 810 |
| M7 | 504 | 280 | 560 |
| M6 | 324 | 180 | 360 |
| M5 | 252 | 140 | 280 |
| M4 | 216 | 120 | 240 |
| M3 | 144 | 80 | 160 |
| M2 | 144 | 80 | 160 |
| M1 | 144 | 80 | 160 |

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# Encoded & Decoded Multiplexer



➤ **Change in transistor size**

**1x**

**1x**

**6x**

**6x**
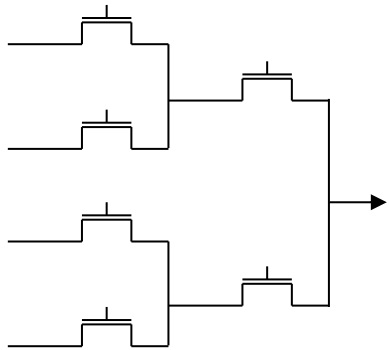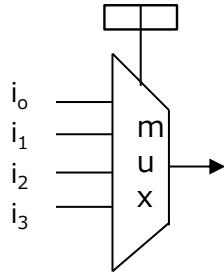
4:1 encoded mux    4:1 decoded mux
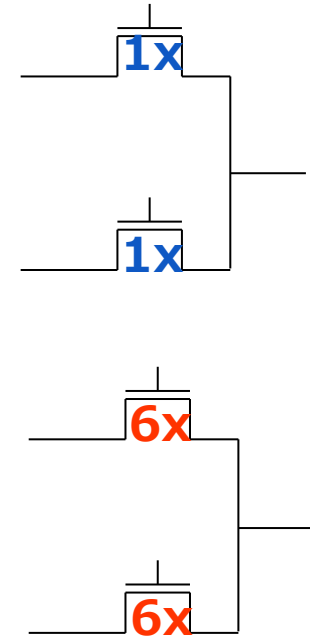
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# Multiplexers – 1x transistor size

**VPR**

### Total Layout Area  Comparision Transistor     weff=1

■VPR -2metals   ■VPR -3metals   ■COFFE - 2metals   ■COFFE- 3metals



**Difference**

(Bar chart categories: 2- LUTor 4:1 dmux, 3-LUT, 4-LUT, 8:1 dmux; y-axis from 0% to -80%)
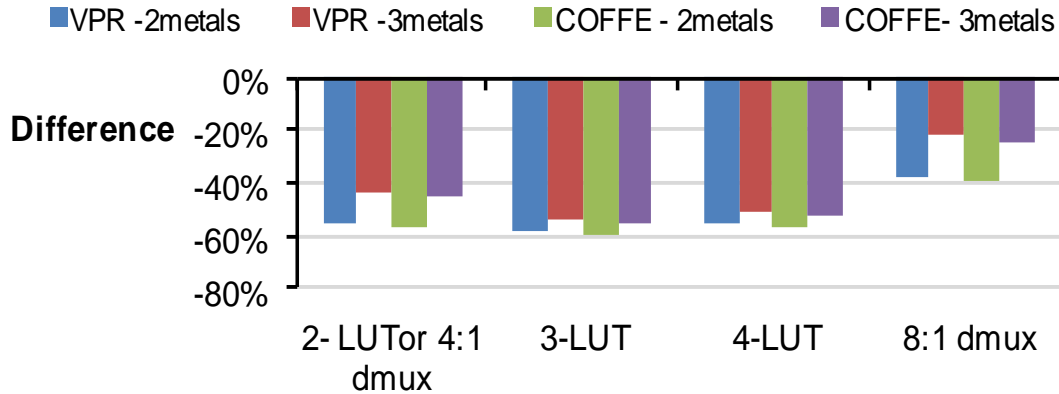
| Metal | Multiplexer Type | min | max | net variation |
|-------|------------------|-----|-----|---------------|
| **2 metal** | **Encoded** | 56% | 59% | 3% |
| | **Encoded & Decoded** | 37% | 59% | **22%** |
| **3 metal** | **Encoded** | 43% | 54% | 11% |
| | **Encoded & Decoded** | 22% | 54% | **32%** |

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# Multiplexers – 1x transistor size

**COFFE**

**Total Layout Area Comparision Transistor     weff=1**

■ VPR -2metals   ■ VPR -3metals   ■ COFFE - 2metals   ■ COFFE- 3metals

**Difference**
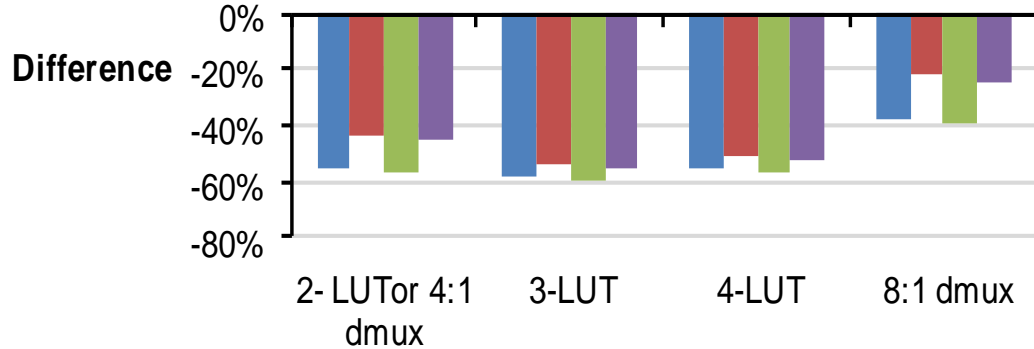


| Metal | Multiplexer Type | min | max | net variation |
|-------|------------------|-----|-----|---------------|
| 2 metal | **Encoded** | 57% | 60% | 3% |
| | **Encoded & Decoded** | 39% | 60% | **21%** |
| 3 metal | **Encoded** | 45% | 56% | 11% |
| | **Encoded & Decoded** | 25% | 56% | **31%** |

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# Effect of transistor size

**VPR**

### Total Layout Area Comparision - Transistor weff=6

■ VPR -2metals  ■ VPR -3metals  ■ COFFE - 2metals  ■ COFFE- 3metals

Difference

| Metal | Multiplexer Type | min | max | net variation |
|---|---|---|---|---|
| 2 metal | Encoded 1x | 56% | 59% | 3% |
| | Encoded & Decoded 1x | 37% | 59% | 22% |
| | **Encoded & Decoded 6x** | **-59%** | **18%** | **77%** |
| 3 metal | Encoded 1x | 43% | 54% | 11% |
| | Encoded & Decoded 1x | 22% | 54% | 32% |
| | **Encoded & Decoded 6x** | **-54%** | **31%** | **85%** |

# Effect of transistor size

**COFFE**



**Total Layout Area Comparision - Transistor weff=6**

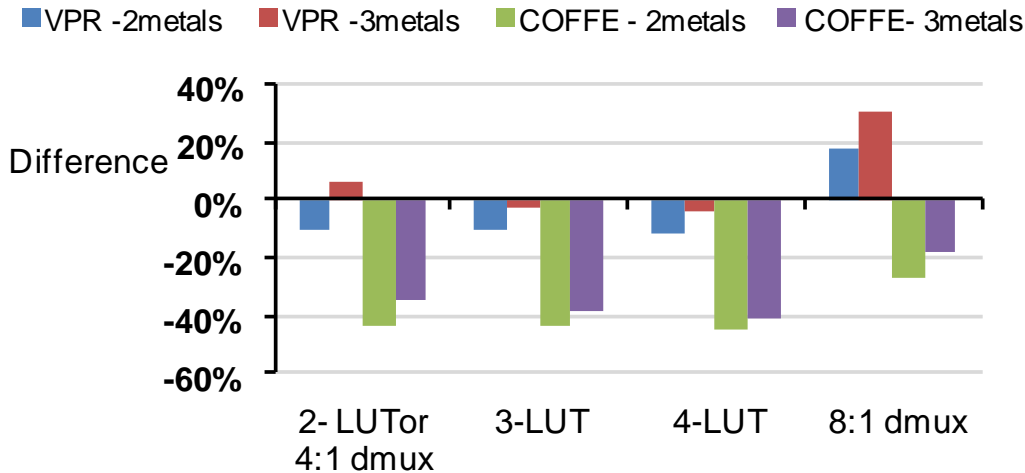Legend: ■ VPR -2metals  ■ VPR -3metals  ■ COFFE - 2metals  ■ COFFE- 3metals

Y-axis: Difference — 40%, 20%, 0%, -20%, -40%, -60%

X-axis: 2- LUTor 4:1 dmux, 3-LUT, 4-LUT, 8:1 dmux
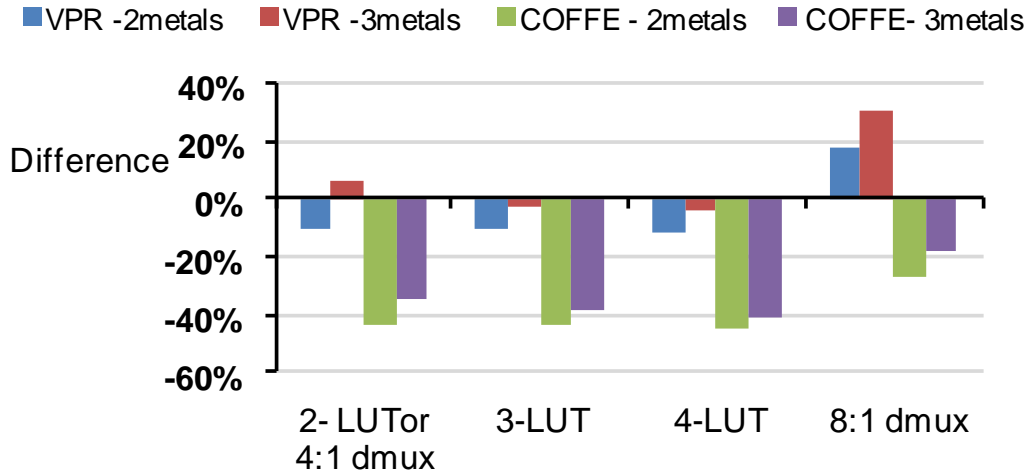
| Metal | Multiplexer Type | min | max | net variation |
|---|---|---|---|---|
| 2 metal | Encoded 1x | 57% | 60% | 3% |
| | Encoded & Decoded 1x | 39% | 60% | **21%** |
| | **Encoded & Decoded 6x** | 27% | 60% | **33%** |
| 3 metal | Encoded 1x | 45% | 56% | 11% |
| | Encoded & Decoded 1x | 25% | 56% | **31%** |
| | **Encoded & Decoded 6x** | 19% | 56% | **37%** |

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# FPGA CMOS Components

**Total Layout Area Comparision - CMOS Components**
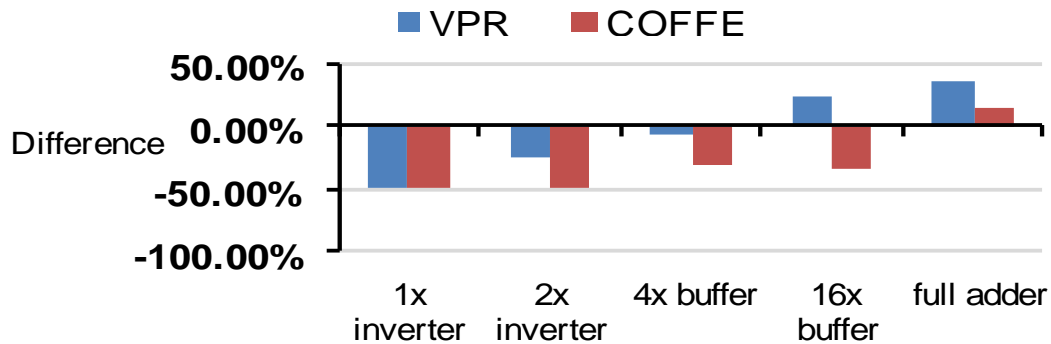


| | min | max | net variation |
|---|---|---|---|
| **VPR** | -50% | 34% | **84%** |
| **COFFE** | -51% | 13% | **64%** |

➢**circuit topology** and **wiring demand** differs for CMOS components

# Conclusion

➢ **Minimum width transistor area model**

- analyzed for commonly used FPGA components

- **VPR** **underestimates :** encoded multiplexers and small size buffers
  **overestimates** : decoded multiplexers with large transistor sizes, large size buffers and full adders.

- **COFFE underestimates** : buffers and encoded and decoded multiplexers
  **overestimates** : full adders.

➢ **Variation in area is due to**

- different components have different circuit topologies

➢ **Accurate FPGA area model**

- consider connectivity and grouping of adjacent transistors

- component by component area model

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# Thank You.

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