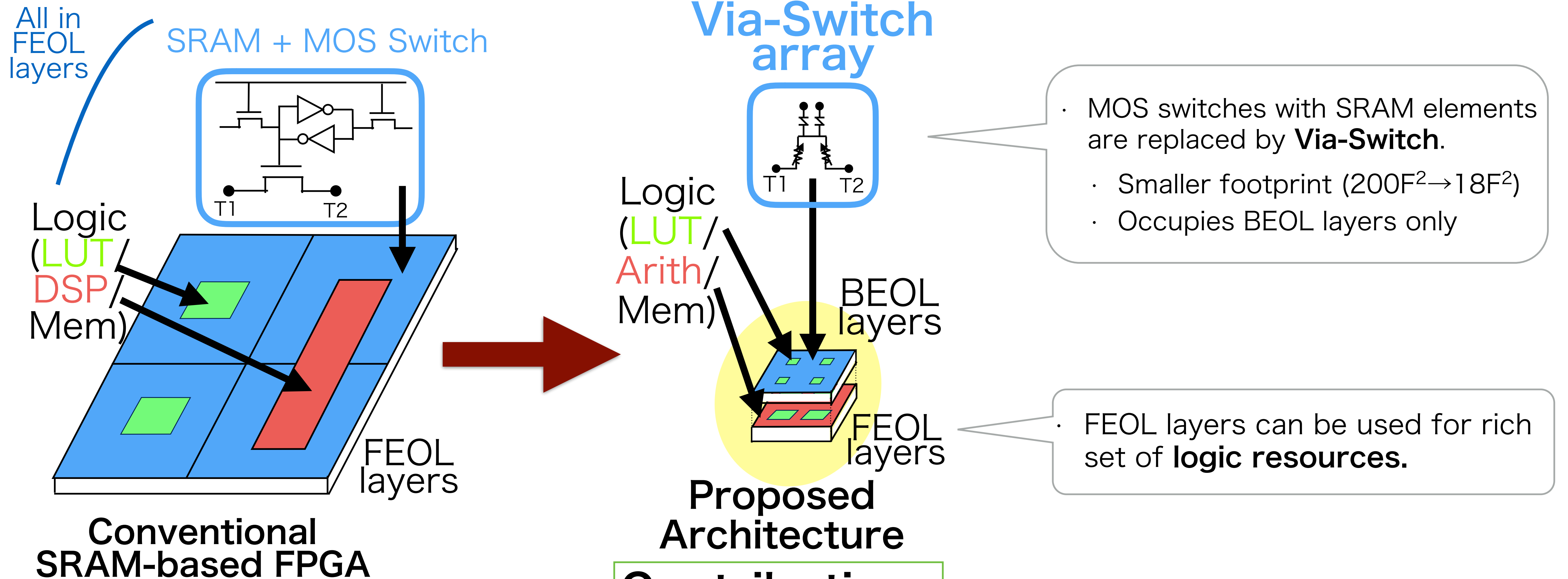


A Highly-dense Mixed Grained Reconfigurable Architecture with Overlay Crossbar Interconnect Using Via-switch

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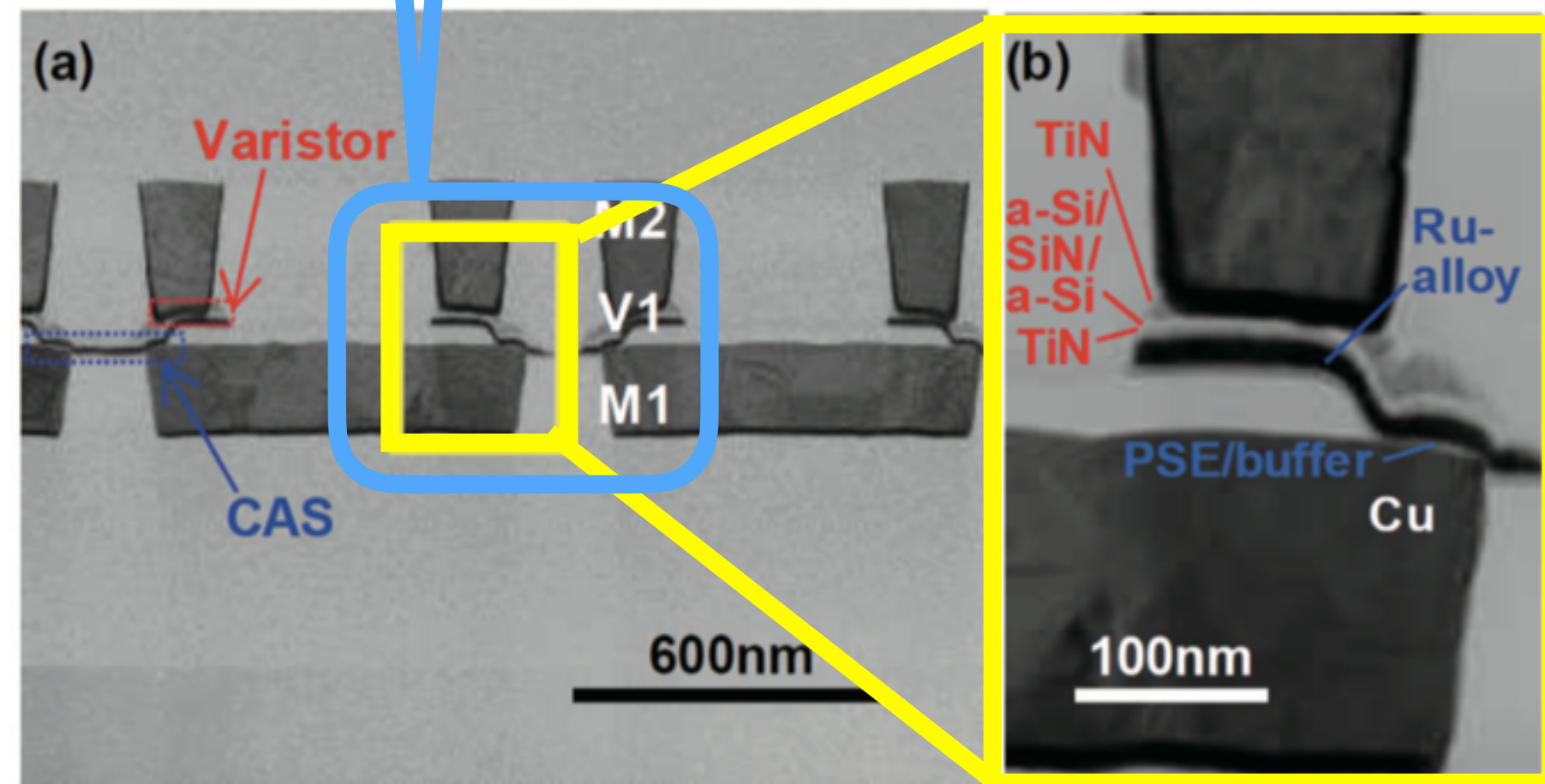
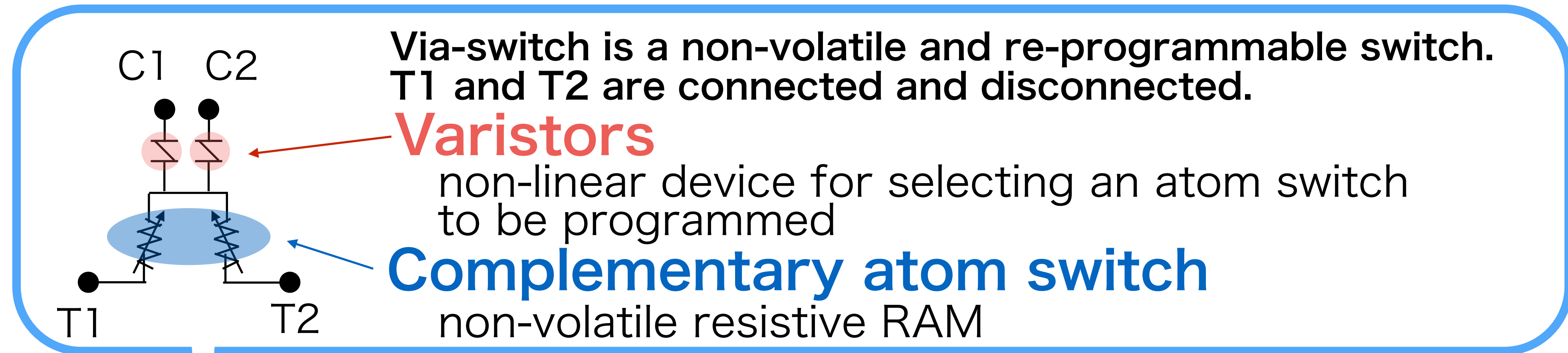
Concepts of Proposed Architecture



Contributions

Crossbar density	Chip area	Delay	Energy
26X	-76%	-90%	-93%

Via-Switch

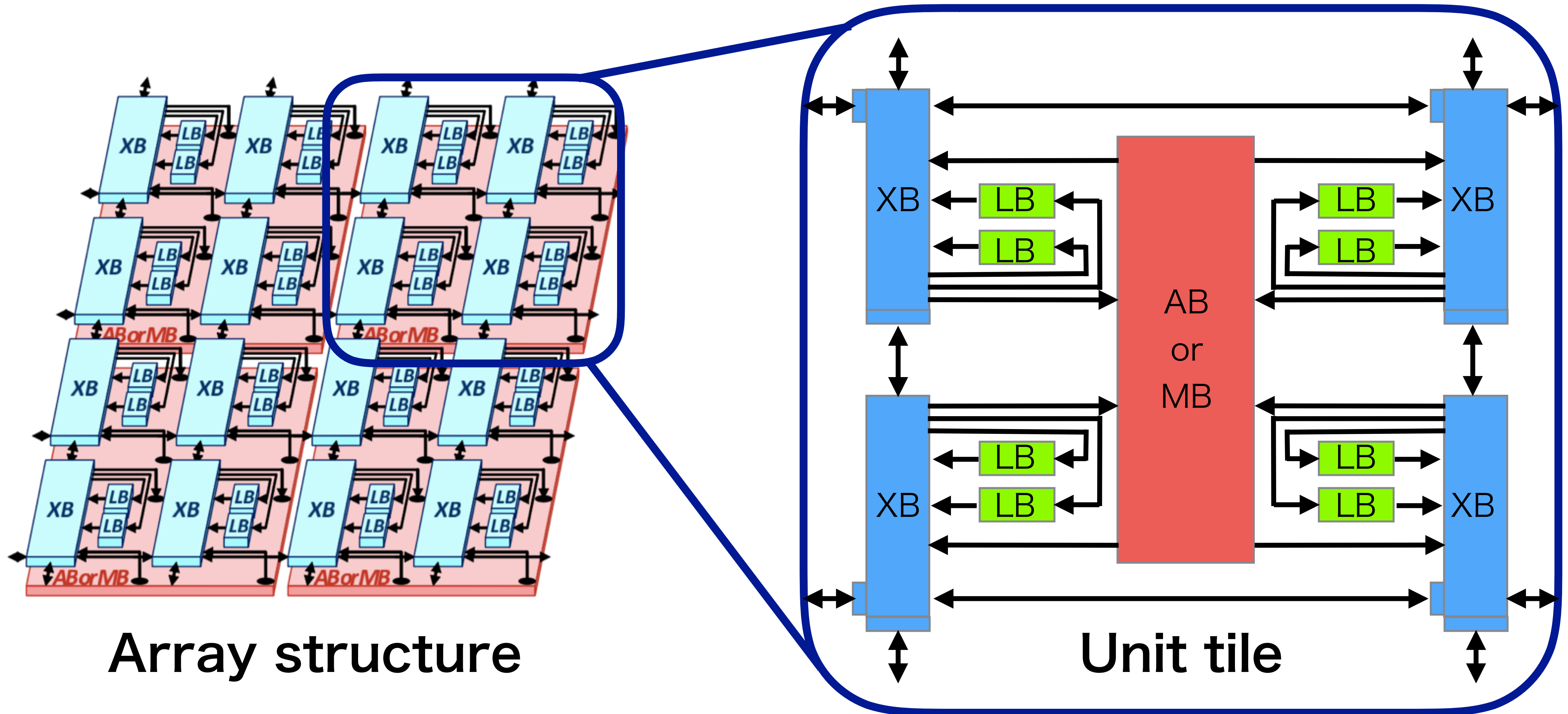


<Features>

- ① Small footprint (6F×3F)
- ② Low resistance (on-R 200Ω)
- ③ Low parasitic capacitance (0.14fF)
- ④ Multi-fanout support

Architecture Overview

The proposed architecture is a homogeneous array of unit tiles

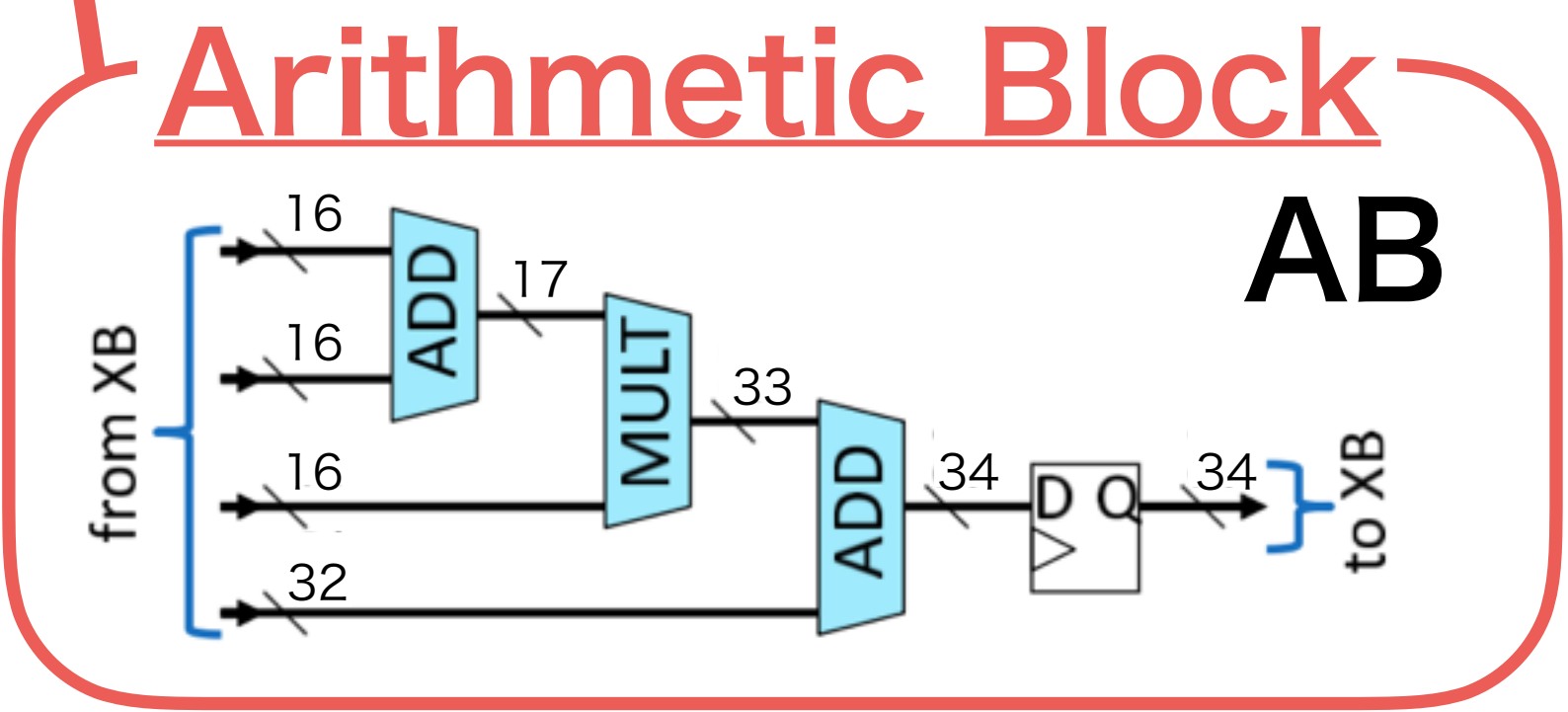
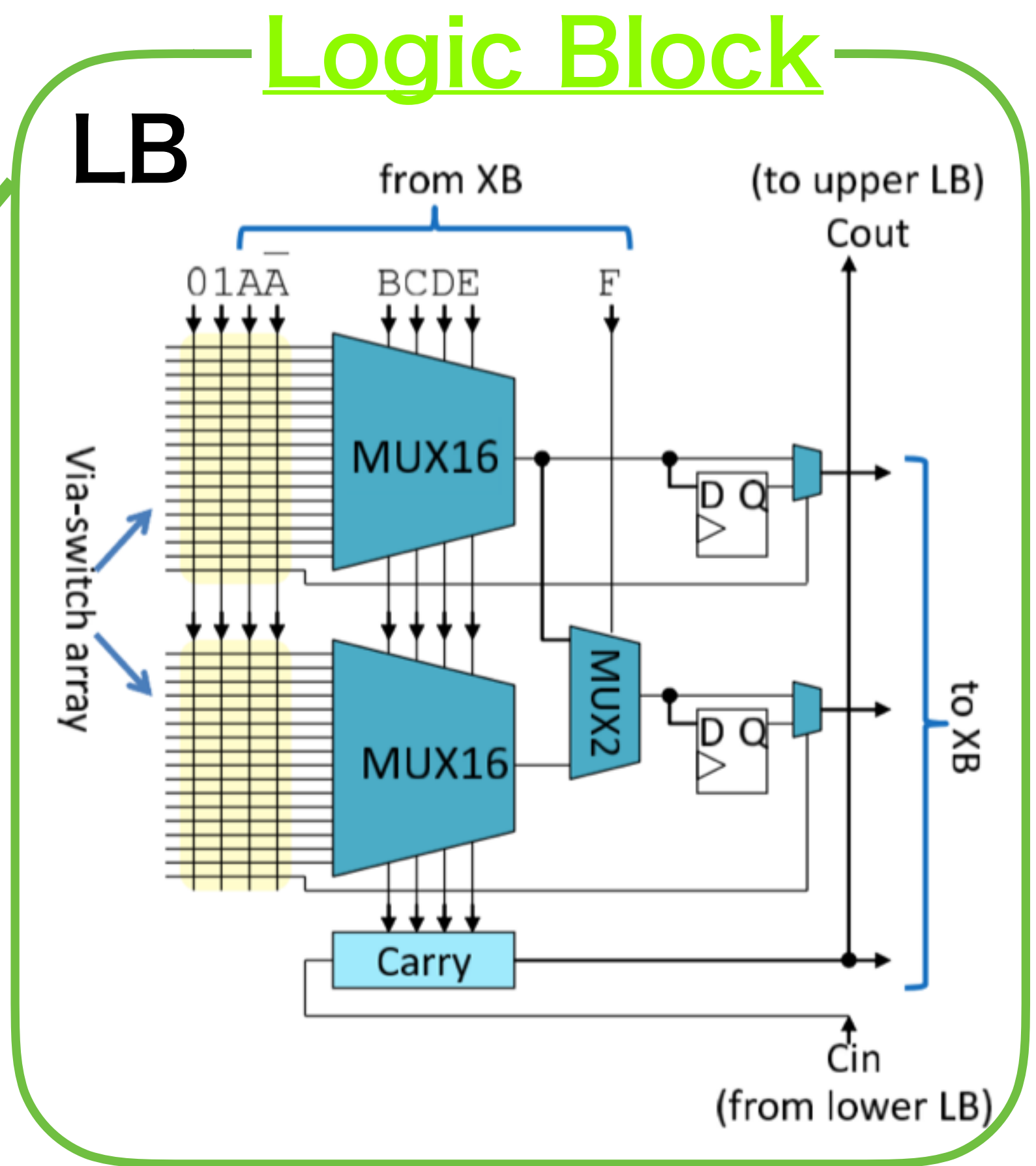
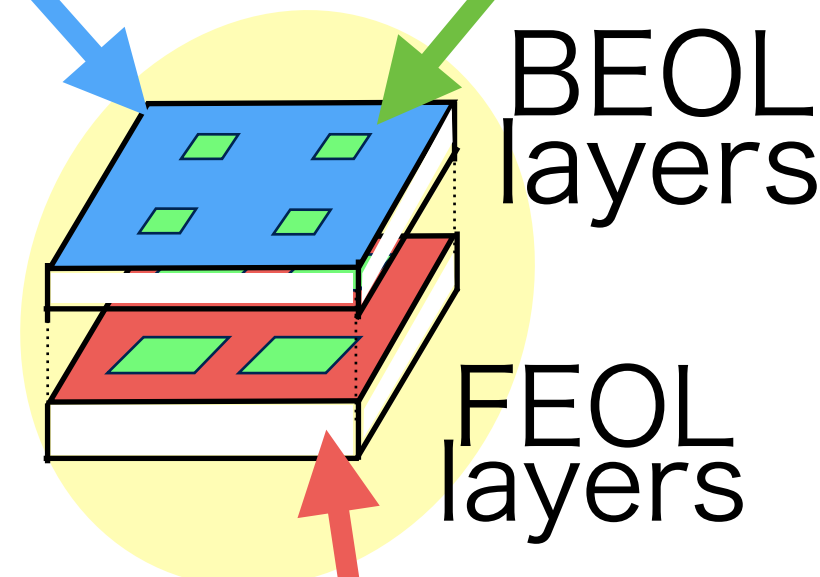
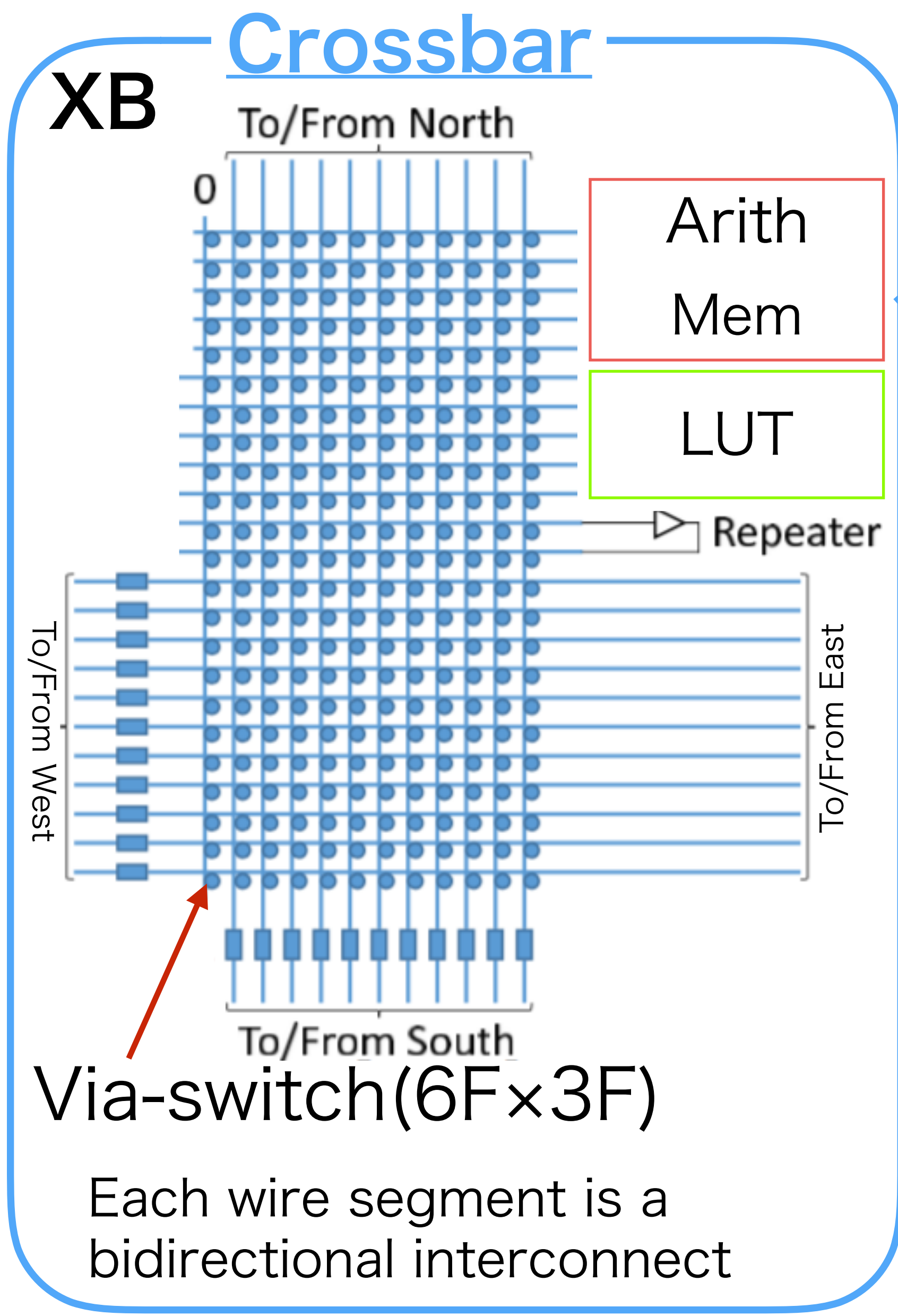


Array structure

Unit tile

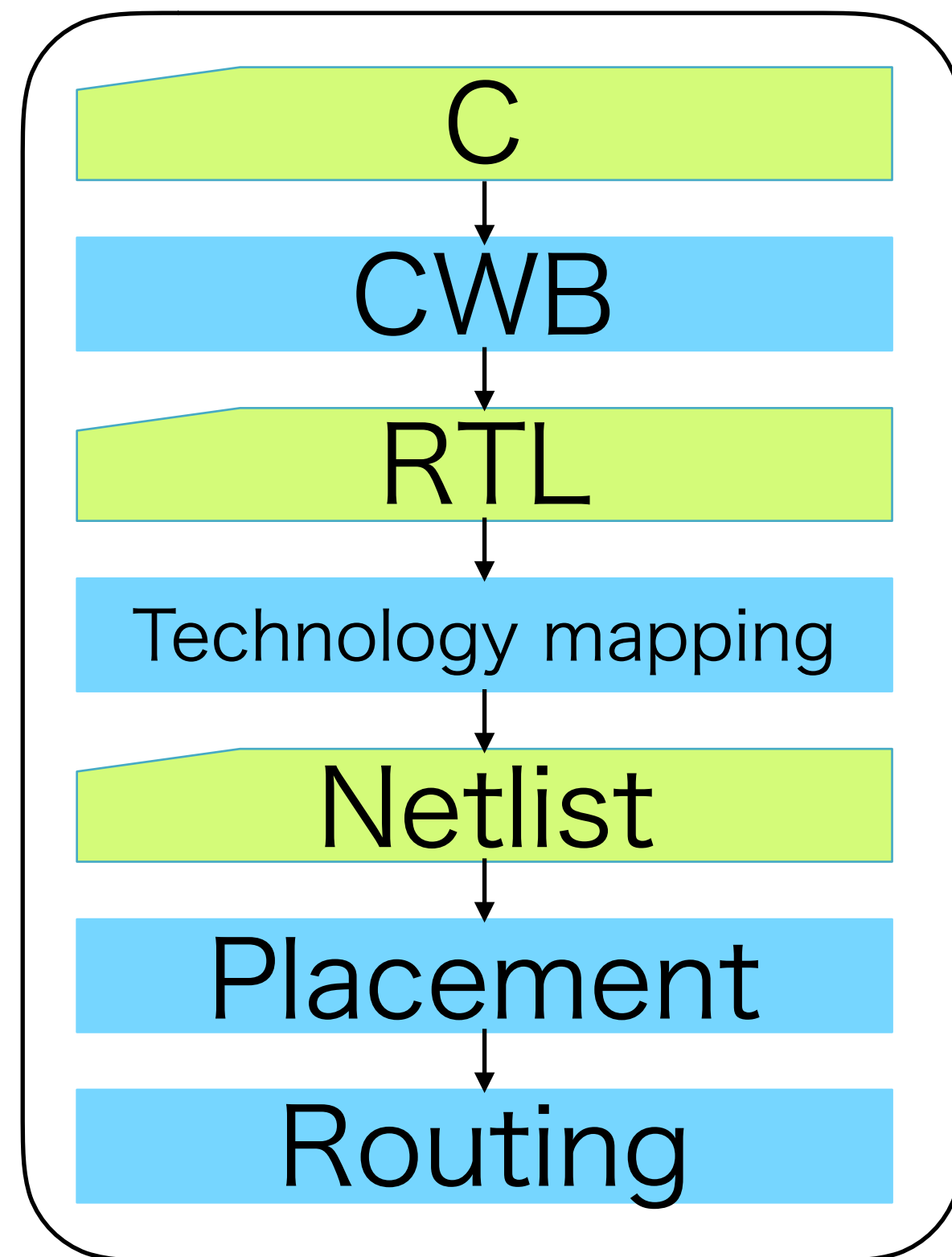
The unit tile consists of four crossbar blocks (XBs), eight fine-grained logic blocks (LBs) and a coarse-grained arithmetic block (AB) or memory block (MB).

Architecture Components



Mapping Experiments

<Design Flow>



<Target Design>

We implemented a design “**CConv**”, a front-end circuit for image sensor including RGB-YUV conversion

Required logic resources for “CConv”

Target Architecture	AB	LB	Unit tile array size
FGRA	—	512	8×8 (512LB)
MGRA (proposed)	14	76	4×4 (16AB+128LB)

Results

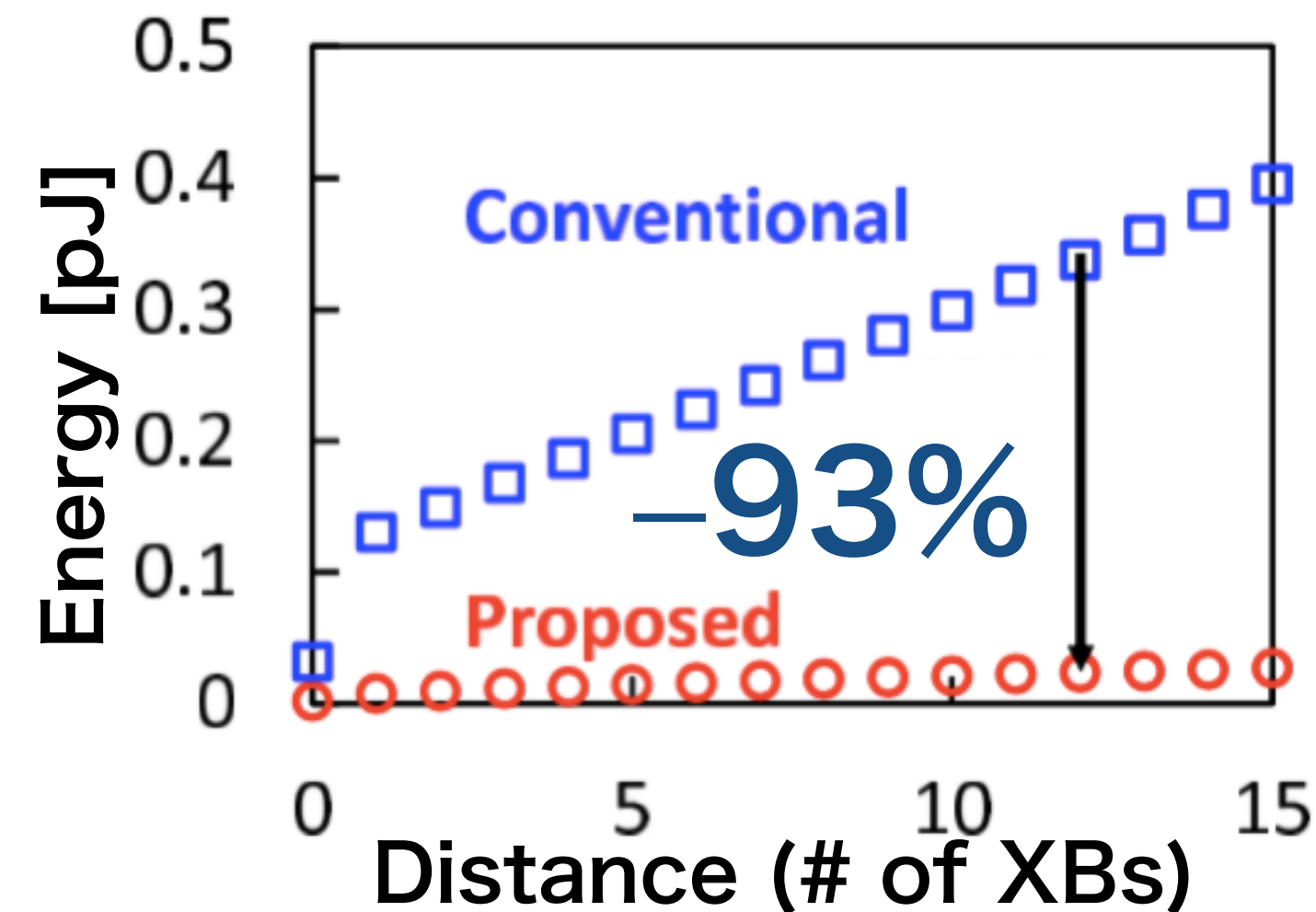
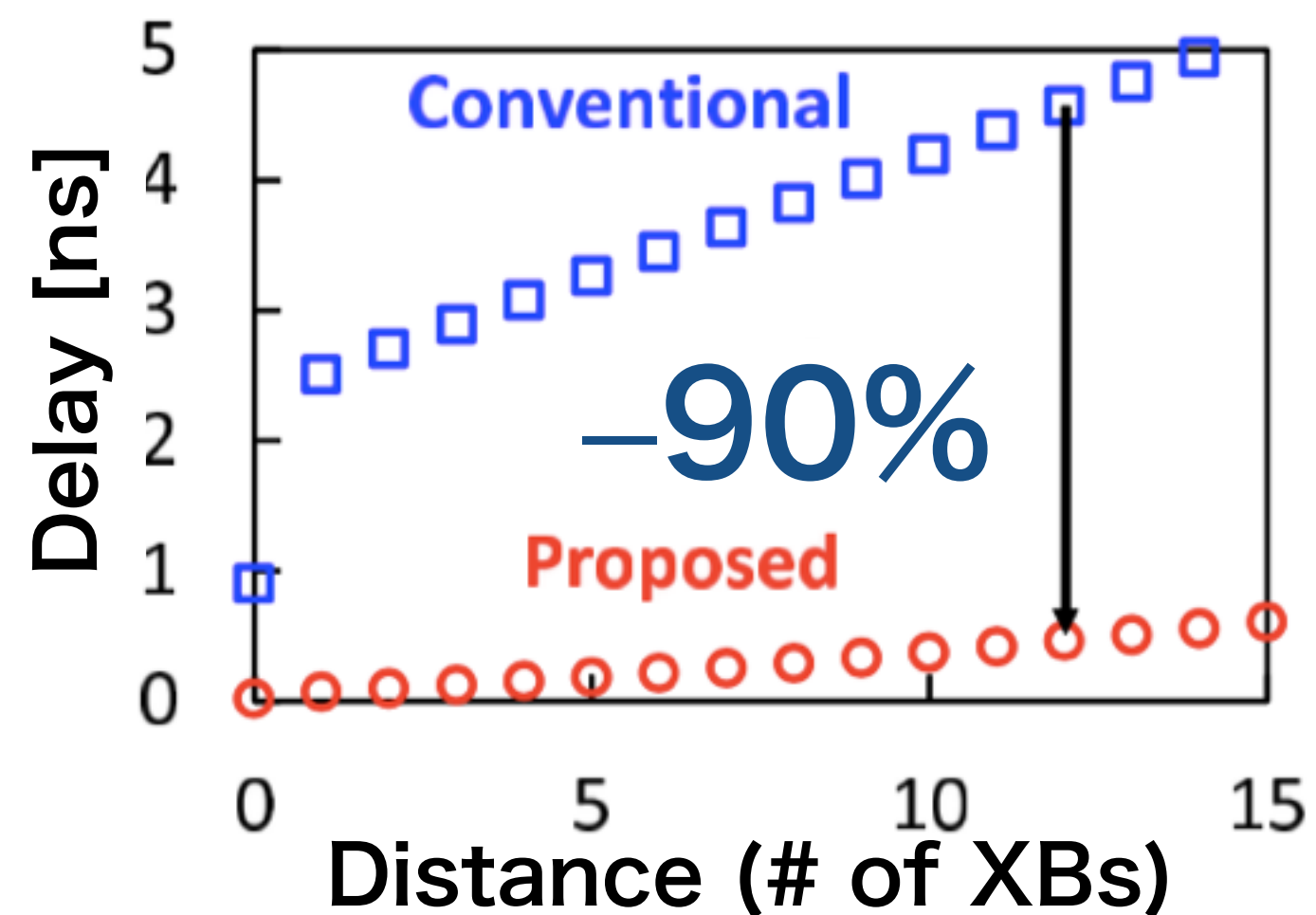
(1) Array Area

Comparison of the array area needed for implementing “CConv”

Architecture	Track	BEOL area	FEOL area	Tile area	Array size	Array area
FGRA unidir.	68	441kF ²	87kF ²	5508 μm^2	8x8	352512 μm^2
MGRA bidir.	44	308kF ²	426kF ²	5319 μm^2	4x4	85108 μm^2

-76%

(2) Delay and Energy



Circuit simulation result at 0.5V operation using a circuit model of 91x44 crossbar with the equivalent circuit model of the via-switch

This improvement can contribute to filling the gap between FPGA and ASIC.

Thank you!

Please visit my poster.