Stress-Aware Routing to Mitigate Aging Effects in SRAM-based FPGAs

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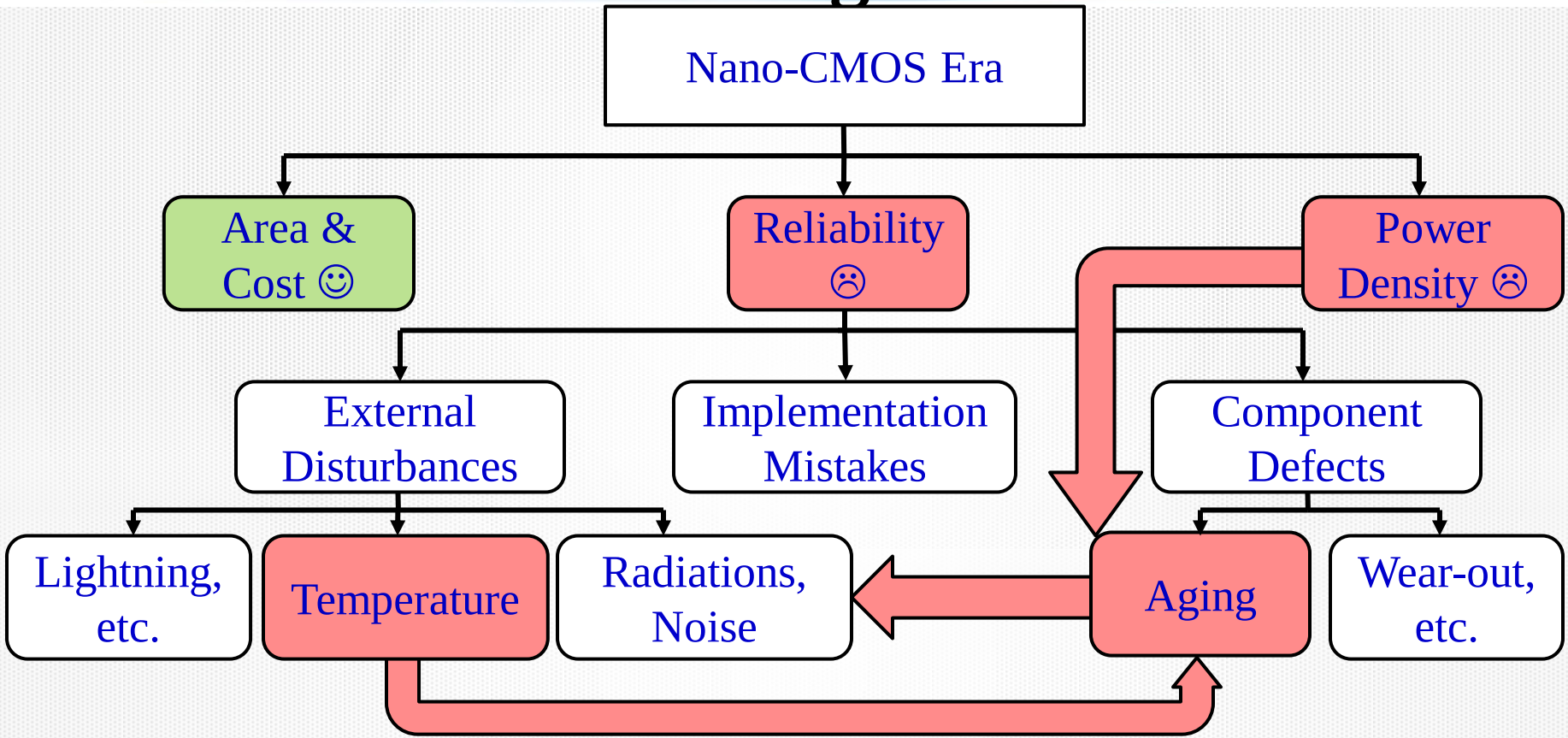
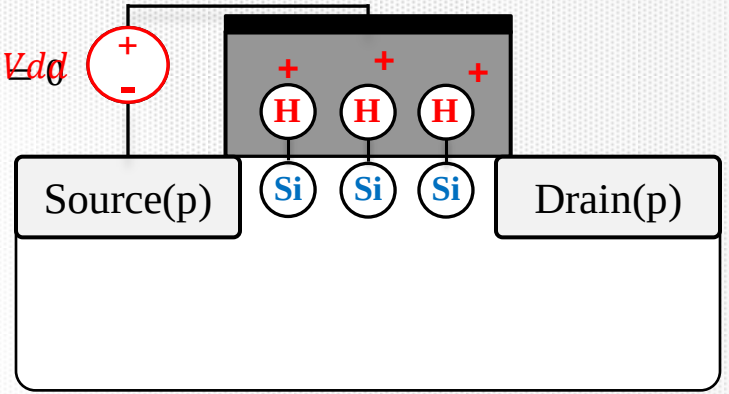
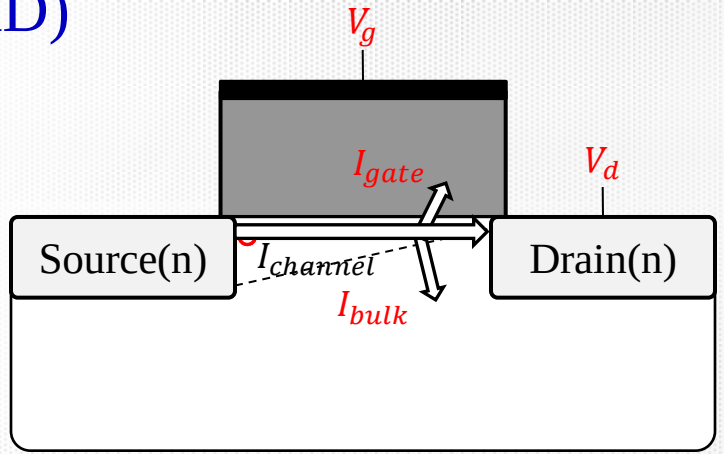
Nano-CMOS Challenges



Basic Concepts: Aging Phenomenon

- Aging
  - Bias Temperature Instability (BTI)
    - Negative BTI ⟶ pMOS type
    - Positive BTI ⟶ nMOS type
  - Hot Carrier Induced Degradation (HCID)
    - Negative HCID ⟶ pMOS type
    - Positive HCID ⟶ nMOS type
  - Other types:
    - Time Dependent Dielectric Breakdown
    - Electro migration



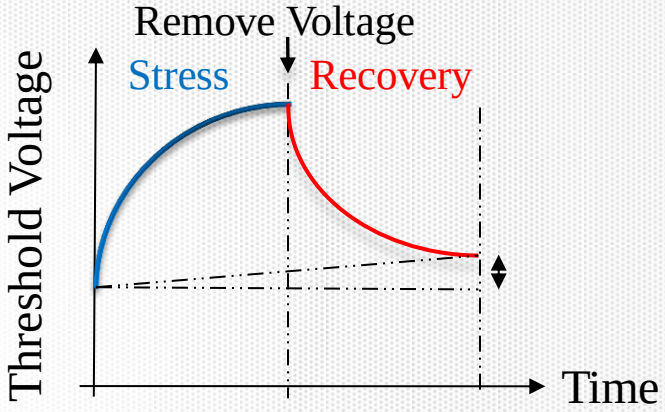


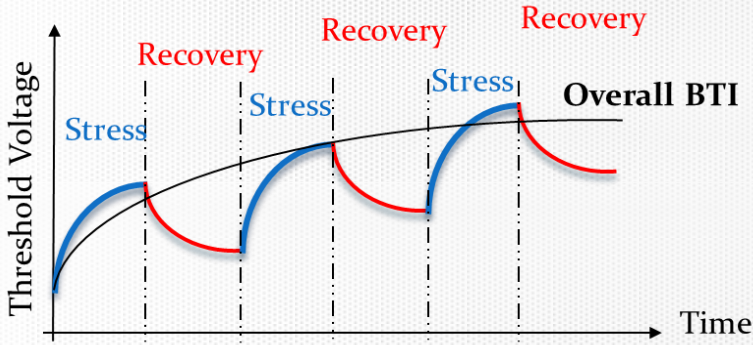
Basic Concepts: BTI

- Bias Temperature Instability
  - Includes two phases:
    - ✦ Stress time
      - Applied voltage to Gate of MOS
      - $|V_{gs}| = V_{dd}$ ➔ Threshold voltage ↑
    - ✦ Recovery time
      - Remove voltage to Gate of MOS
      - $|V_{gs}| = 0$ ➔ Threshold voltage ↓
  - Ideal Duty Cycle (DC) = 0.5

➢ Attention:

$$|\Delta V_{th}|_{Recovery-Time} < |\Delta V_{th}|_{Stress-Time}$$

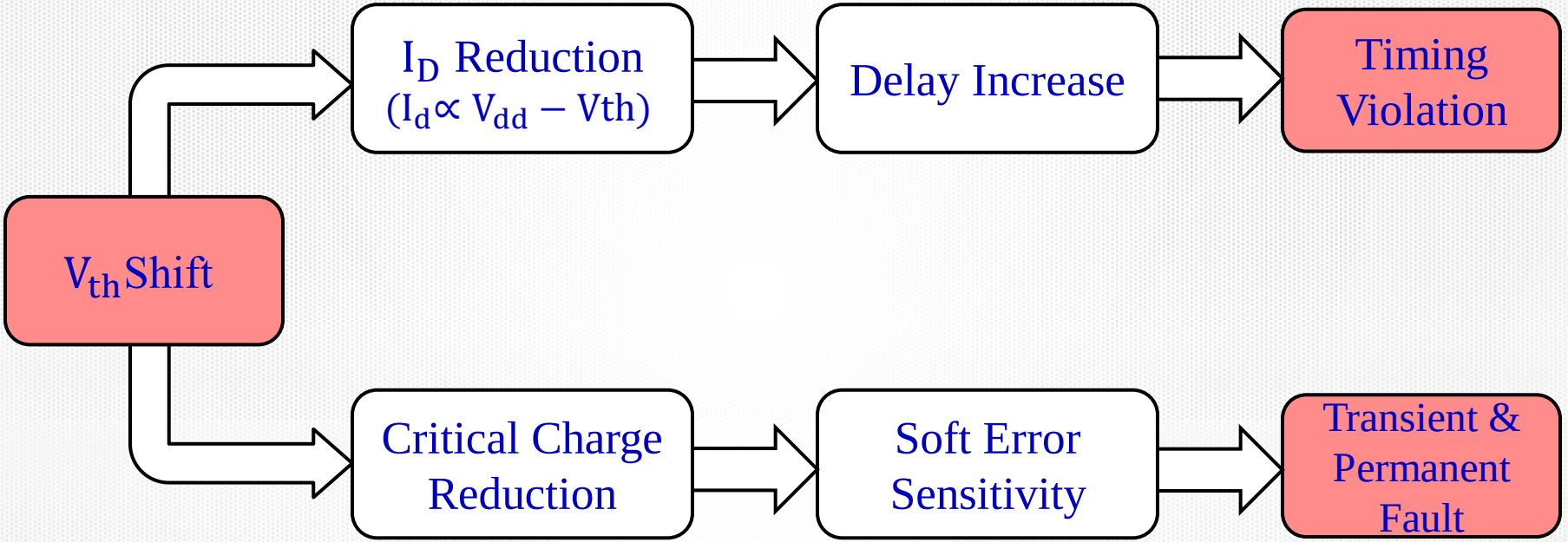




S. Kiamehr, A. Amouri, and M. B. Tahoori, Investigation of nbti and pbti induced aging in different lut implementations, *In Intl. Conference on Field − Programmable Technology (FPT),* 2011.

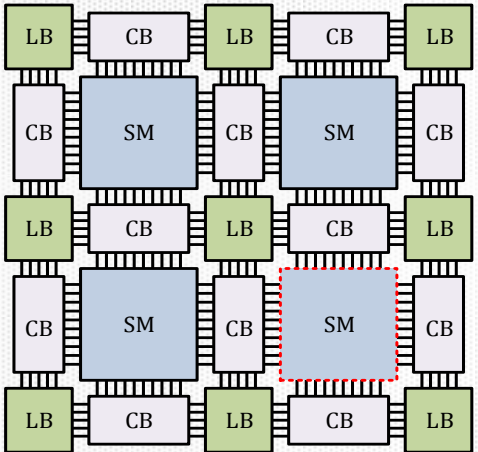
Basic Concepts: BTI Impacts

- Negative Effects of BTI



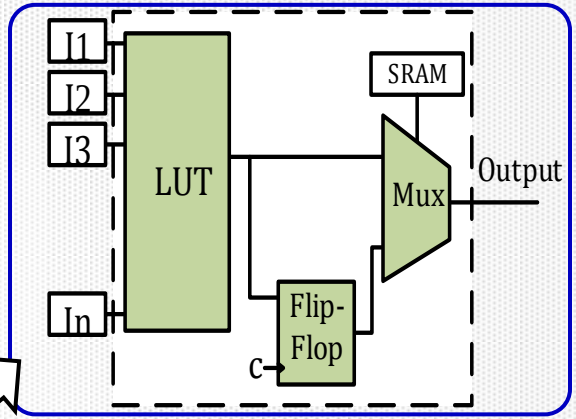
Motivation: FPGA Susceptibility

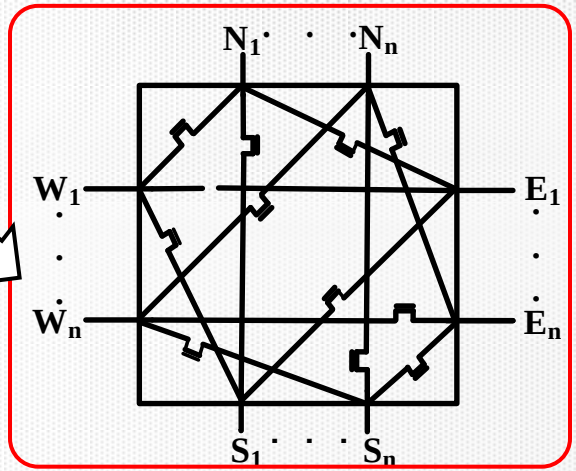
- FPGA High Susceptibility to Aging
  - Circuit varies with each new reconfig.
  - Both logic and configuration memory
    - Configuration memory ➔ permanent fault
  - Too many resources to monitor



Logic: 20%-30%
Routing: 80%-70%

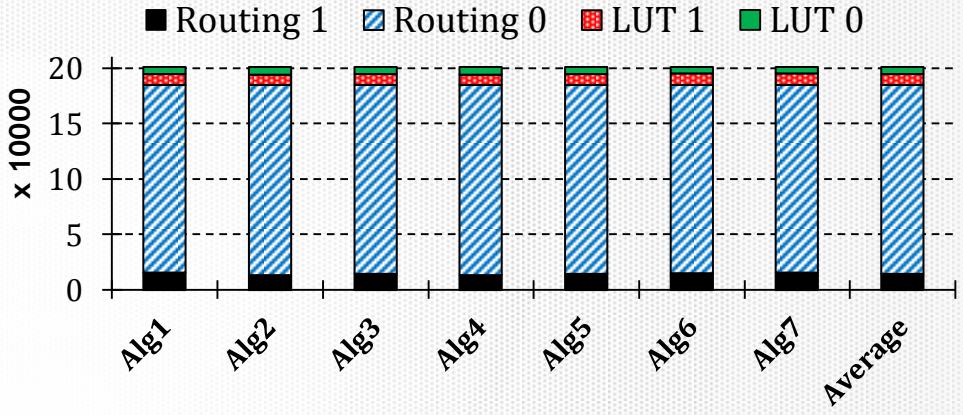
Aging in Routing more Challenging.





Motivation: Routing Vulnerability

Flash Translation Layer Algorithm in SSD Controllers (Min size Virtex-II)

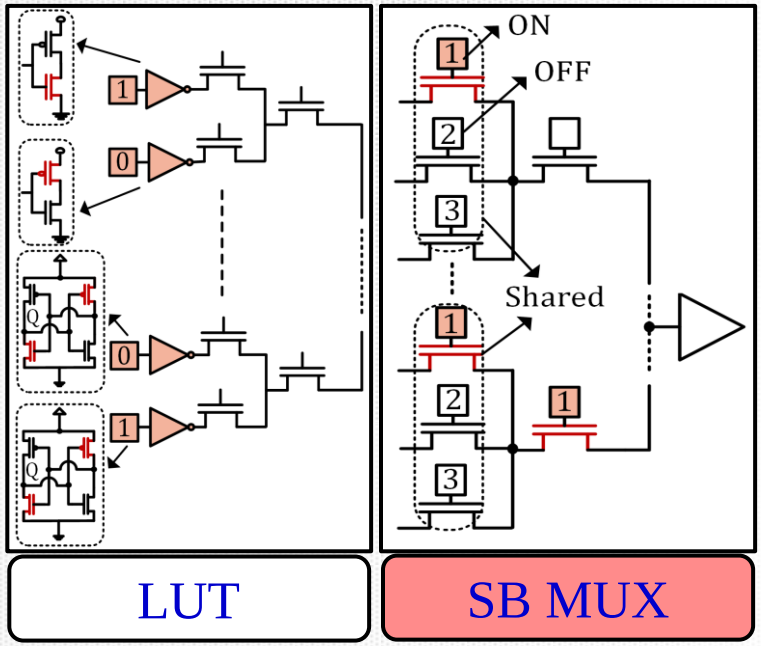


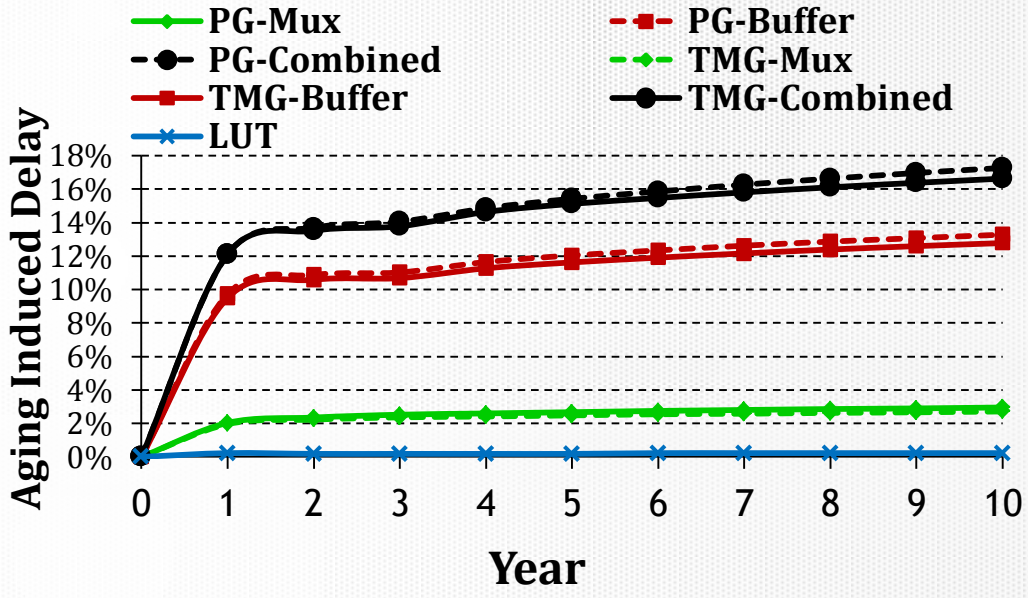
- $P_{stress}(Routing) \approx P_{0\to0} + P_{1\to1} = 0.92 \times 0.92 + 0.08 \times 0.08 = 0.85$

- $P_{stress}(LUT) \approx P_{0\to0} + P_{1\to1} = 0.41 \times 0.41 + 0.59 \times 0.59 = 0.52$

Motivation: Routing Vulnerability

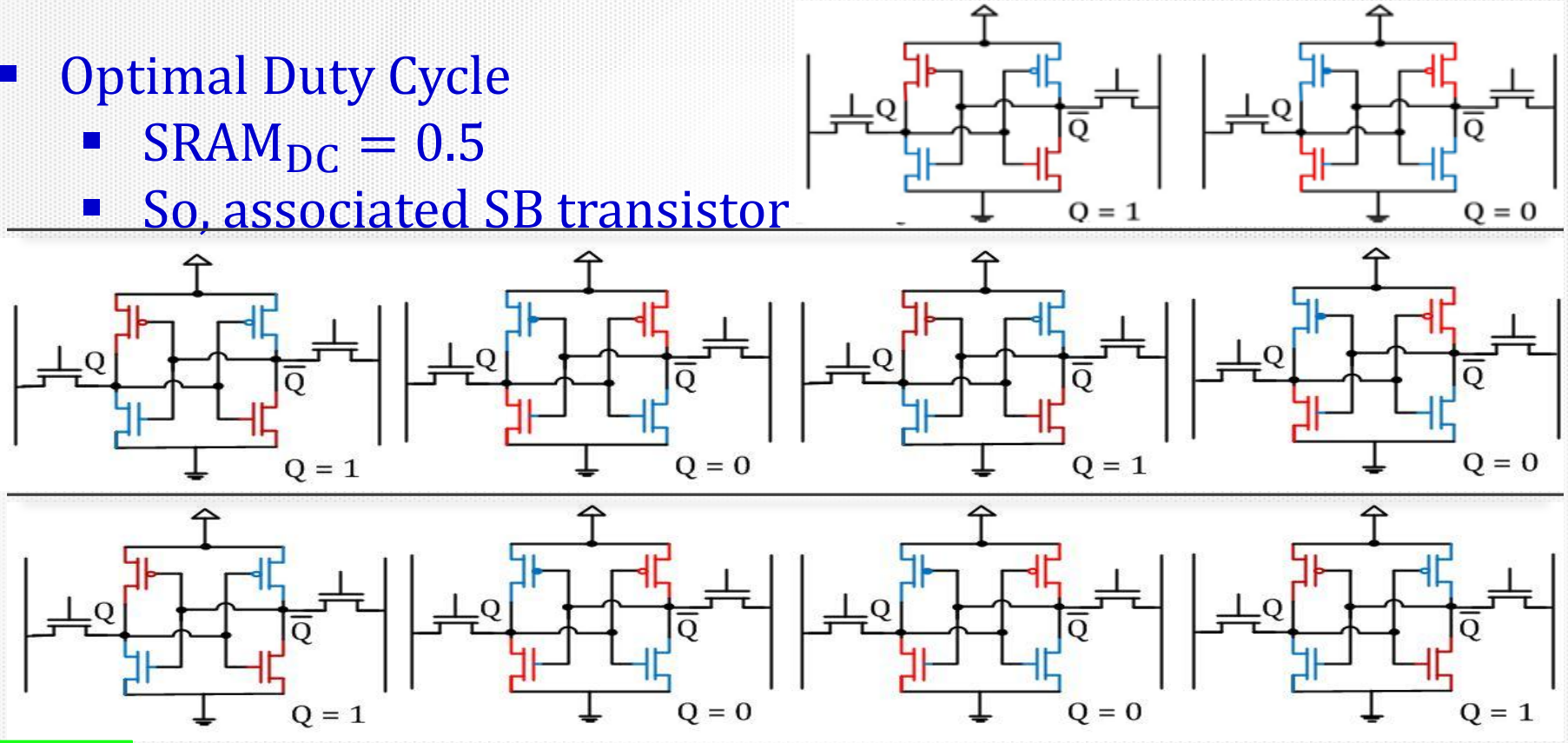
- Routing SRAMs are within Circuit Critical Path
  - Not for LUTs





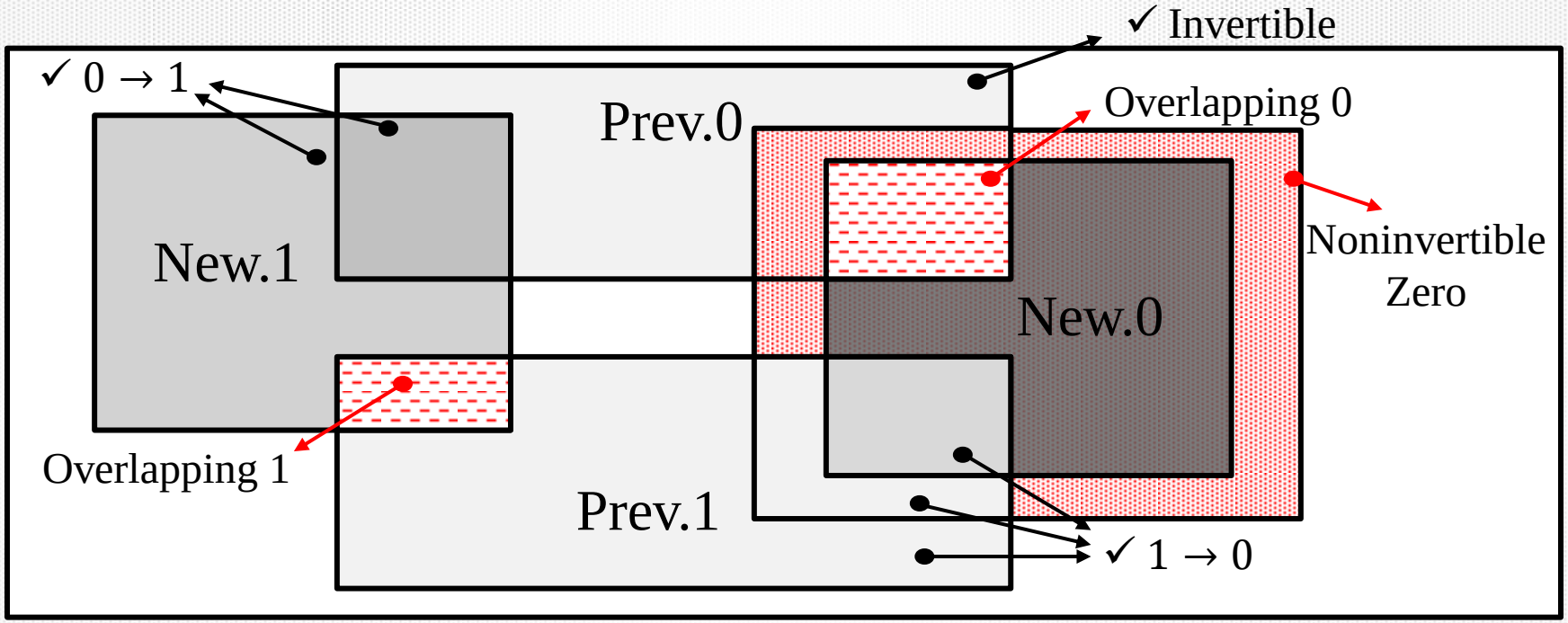
Proposed Method: Duty Cycle

- Optimal Duty Cycle
  - $SRAM_{DC} = 0.5$
  - So, associated SB transistor



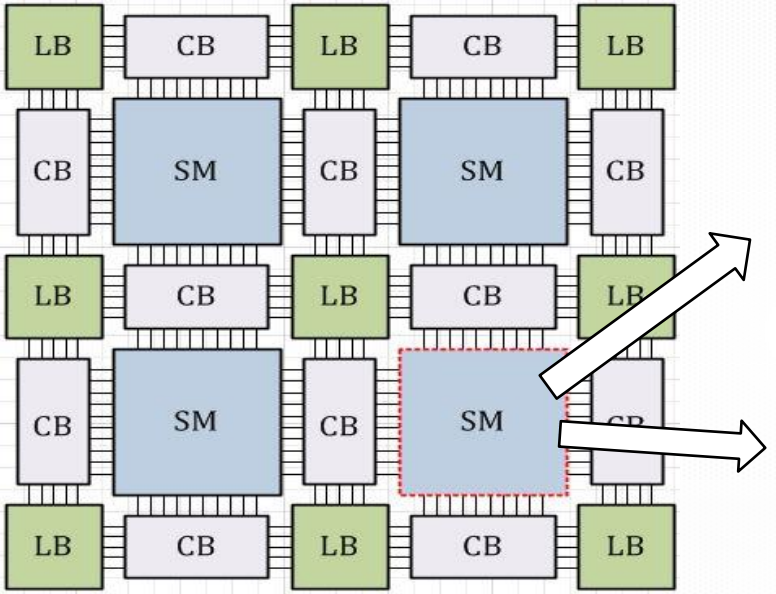
Proposed Method: Reconfigurations

- Configuration Cells in Consecutive Reconfigurations

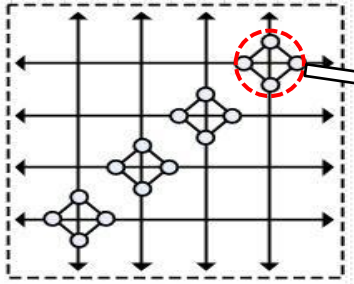


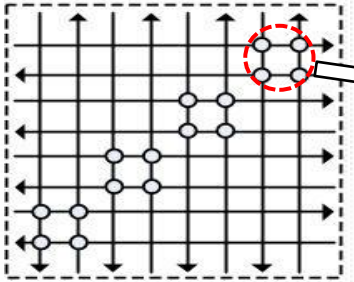
Proposed Method: Base Architecture

- FPGA Architecture and Structures in Proposed Method

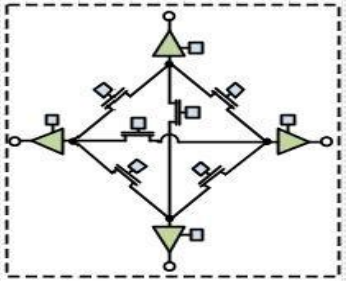


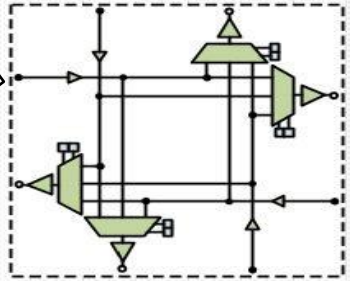
Island-Style Architecture





Bi (top) & Uni-Directional SM (bottom)

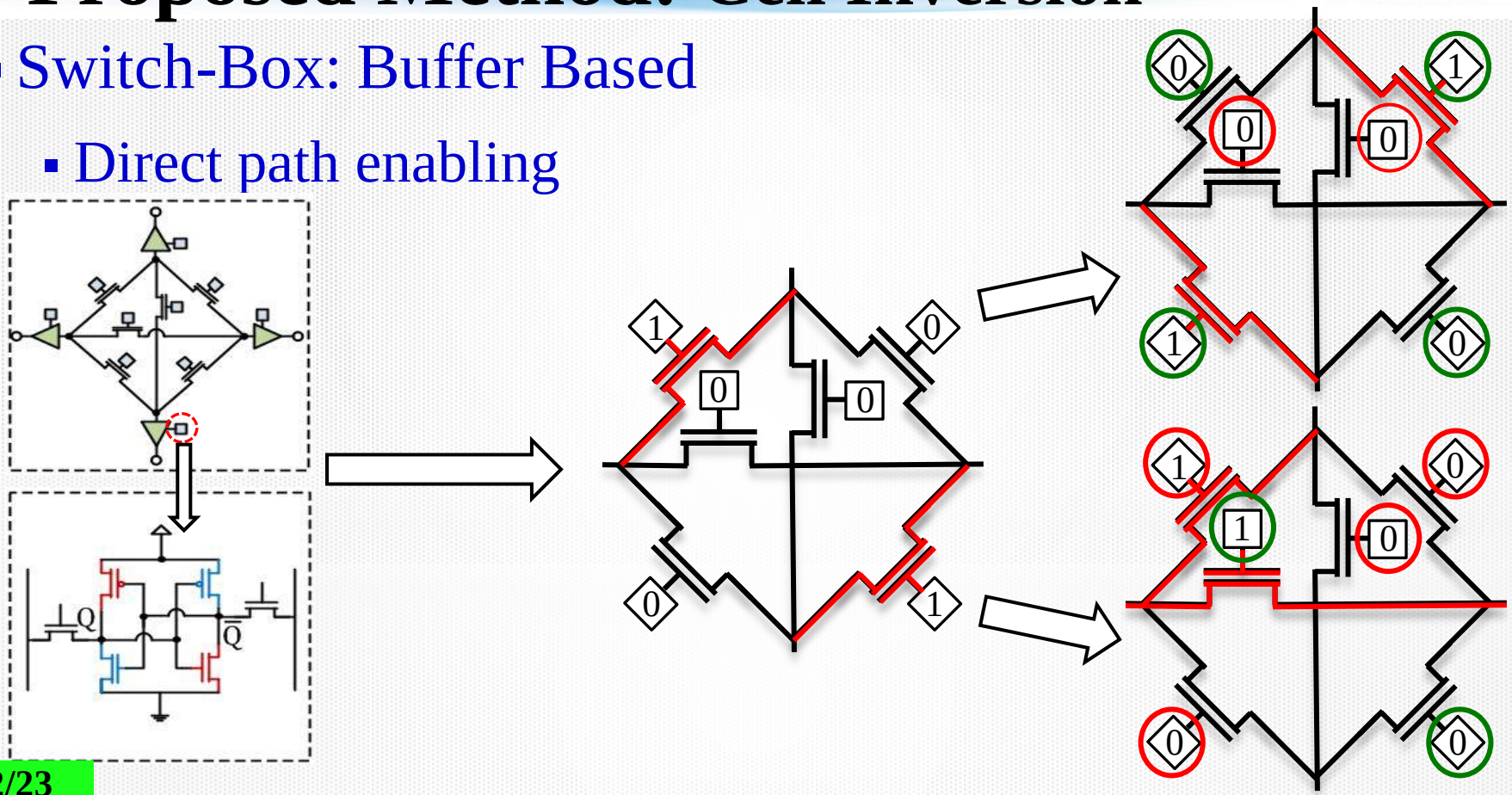




Bi (top) & Uni-Directional SB (bottom)

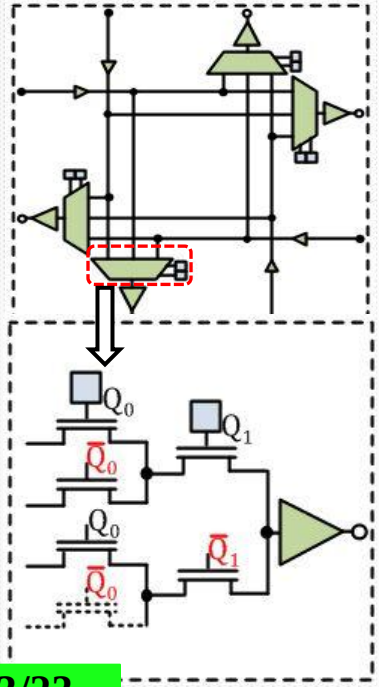
Proposed Method: Cell Inversion

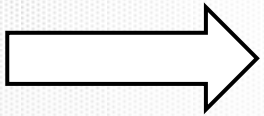
- Switch-Box: Buffer Based
  - Direct path enabling

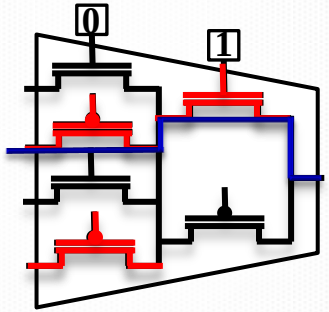


Proposed Method: Cell Inverting

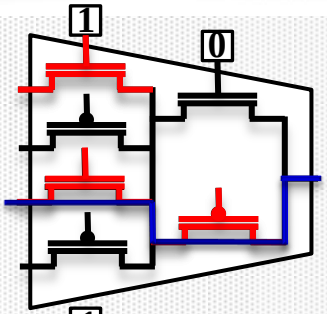
- Switch-Box: Multiplexer Based
  - Hamming distance concept

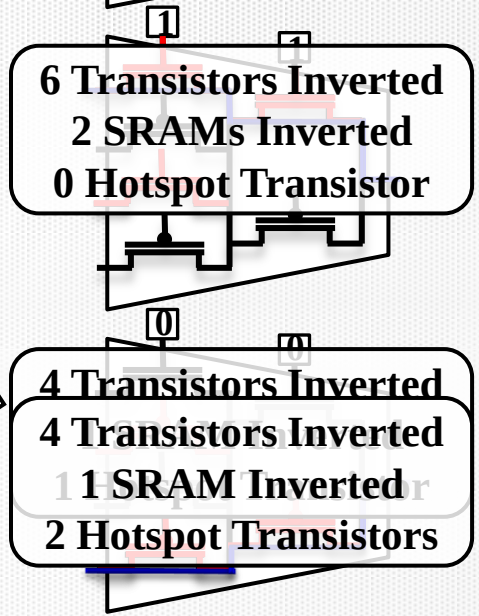






Best Select





Proposed Method

Scheme 1

- Routing by Assigning Higher Cost to Previous Used Cells
- Inverting All Unused Cells

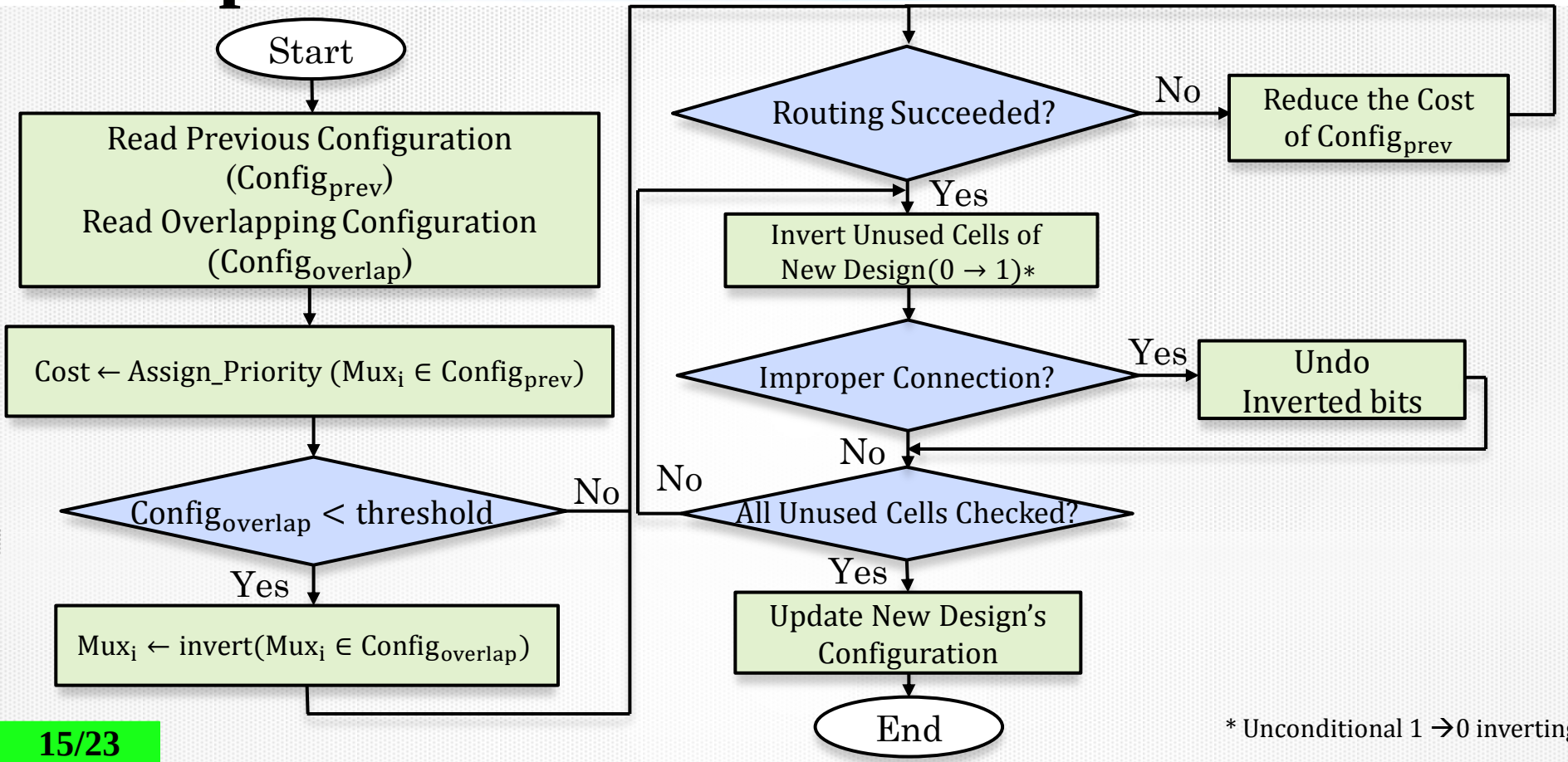
Scheme 2

- Routing by Avoiding Using Previous Active (0 or 1) Cells
- Inverting All Unused Cells

Proposed Method

- Assigning Initial Cost for (prev.) Active SRAMs
- $\text{Overlaping}_{\text{SRAM}} >$ Threshold → Use Scheme 1
- $\text{Overlaping}_{\text{SRAM}} <$ Threshold → Use Scheme 2

Proposed Method: Overall Flow

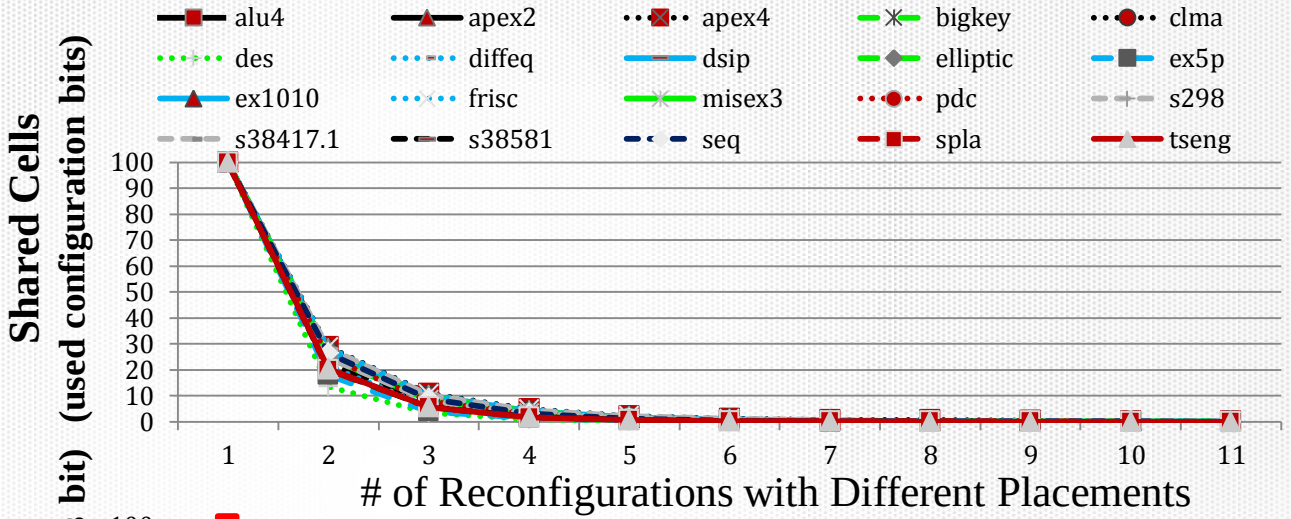


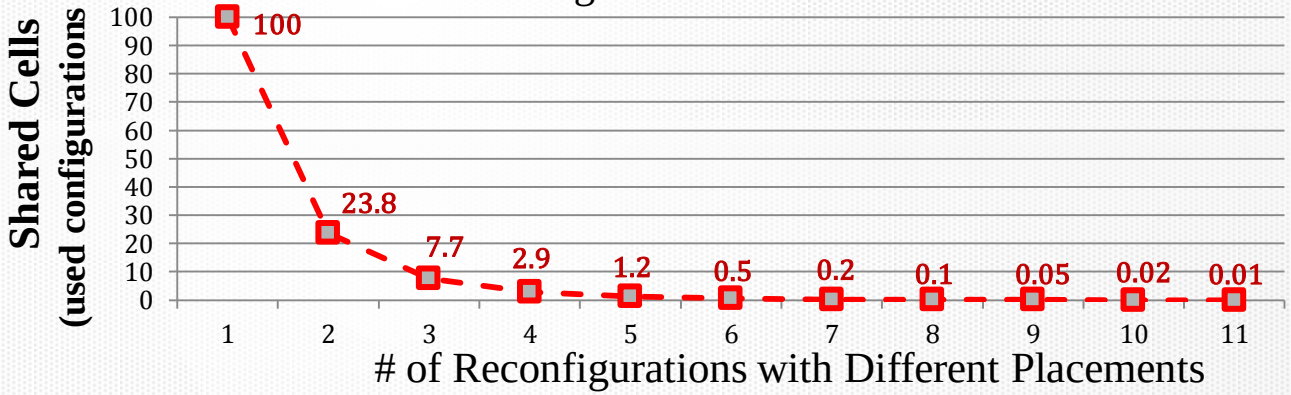
* Unconditional 1 →0 inverting

Proposed Method: Threshold Value

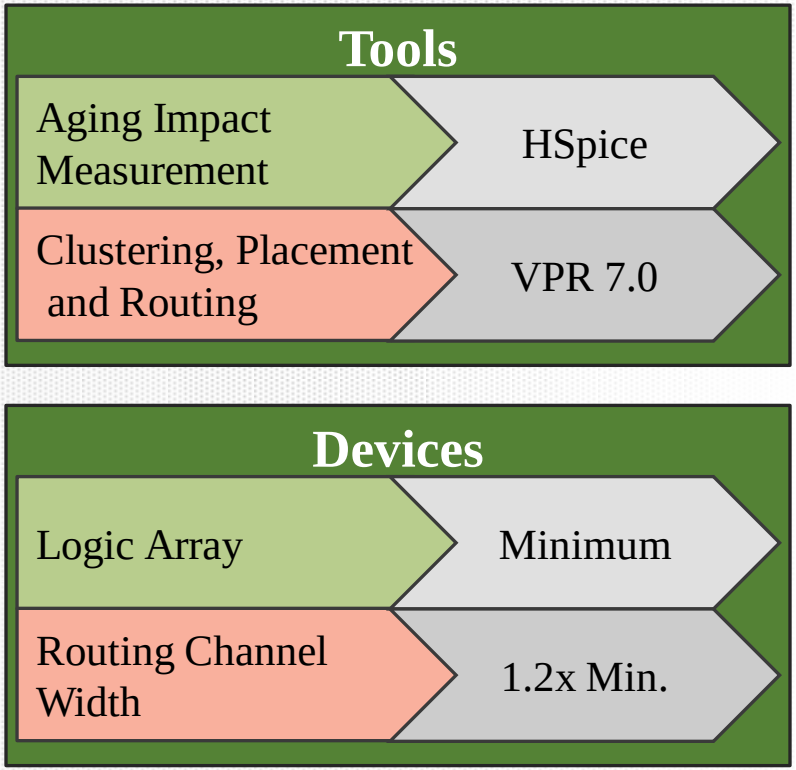
Placing Benchmarks with Different Seed Numbers

Average Overlapping Configuration Bit





Experimental Setup



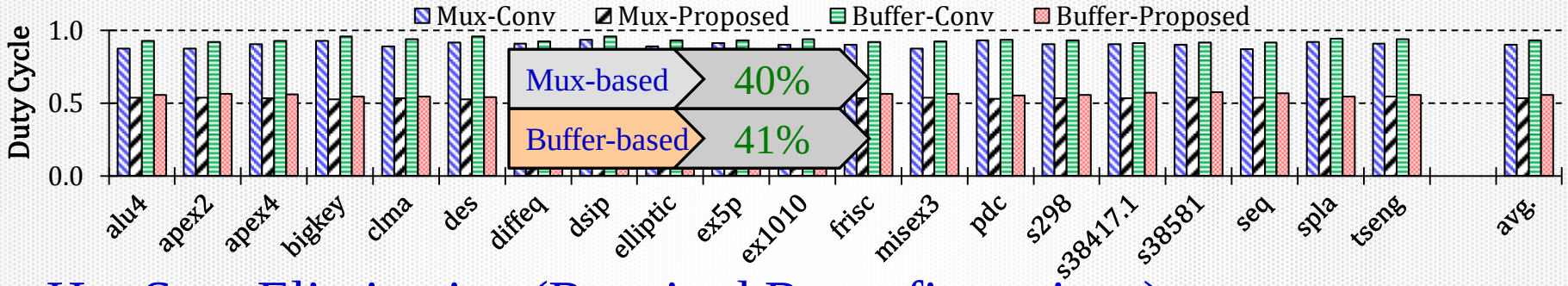
Architecture	Island Style
SB Type	Uni and Bi Directional
Switch Matrix Topology	Subset
SB Structure	Buffer/ Multiplexer
Wire Segment Length	L=1

Experimental Setup (cont.)

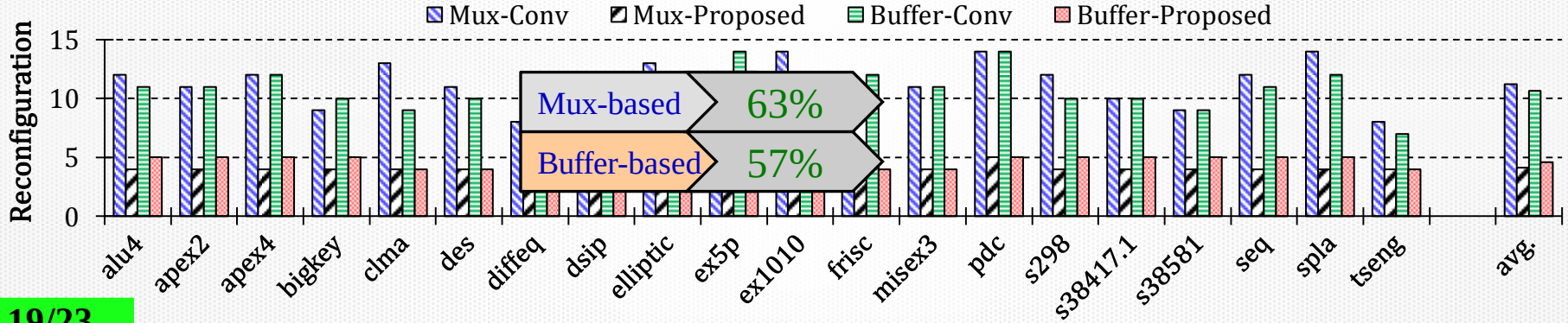
- Assumption
  - Circuits reconfigured in identical time intervals
- Same Circuit is Reconfigured
  - Using different placement seeds
  - FPGA array size and channel width is maintained
  - Same circuit with different placement and routing
    - Analogous to using different circuits
  - VPR tool modified to generate bitstream after routing each circuit

Results

➢Stress Time Reduction (Duty Cycle)

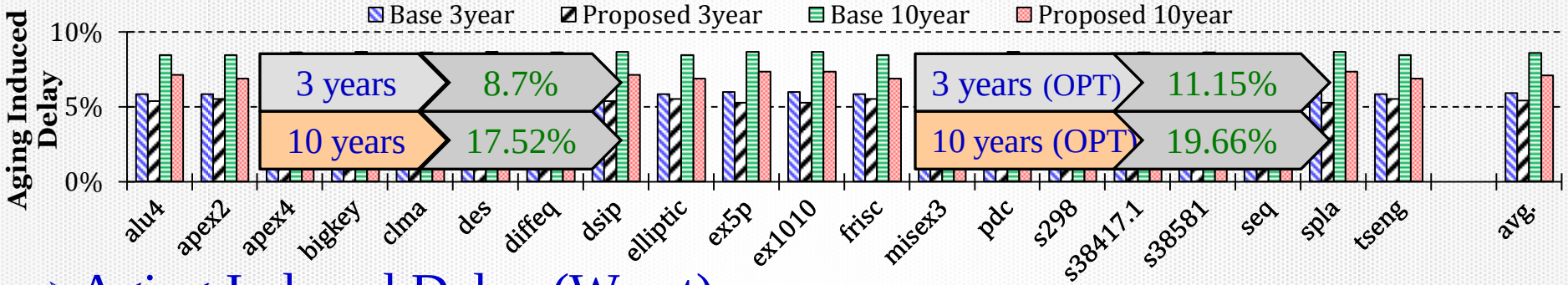


➢Hot Spot Elimination (Required Reconfigurations)

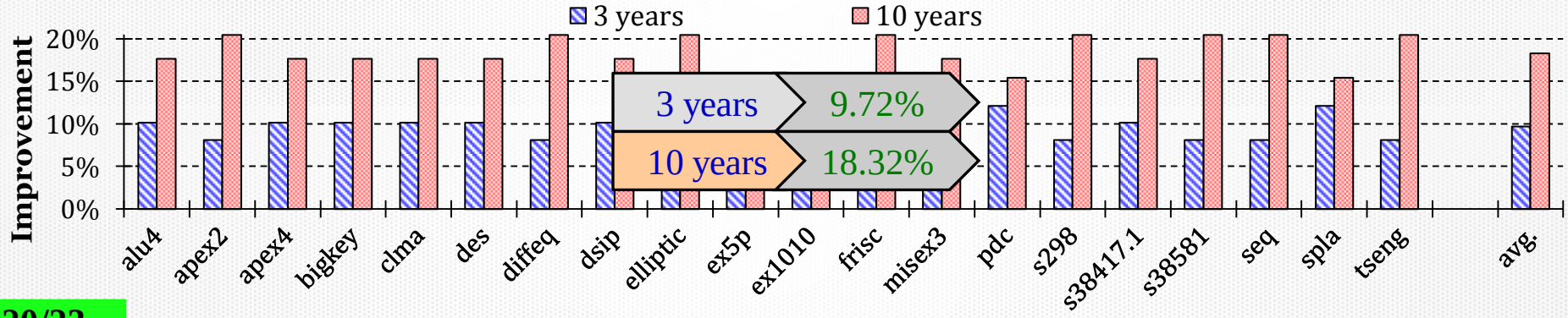


Results (cont.)

➢Aging Induced Delay (Average)

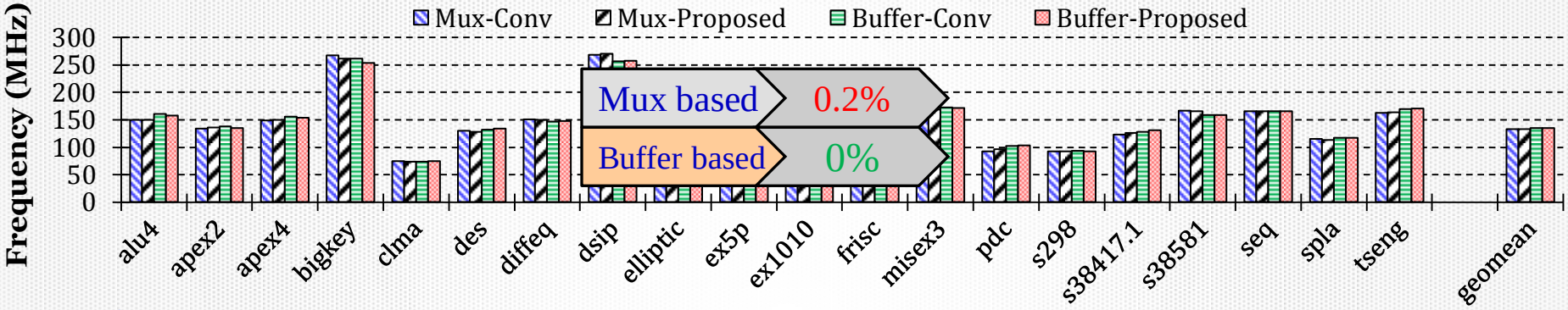


➢Aging Induced Delay (Worst)

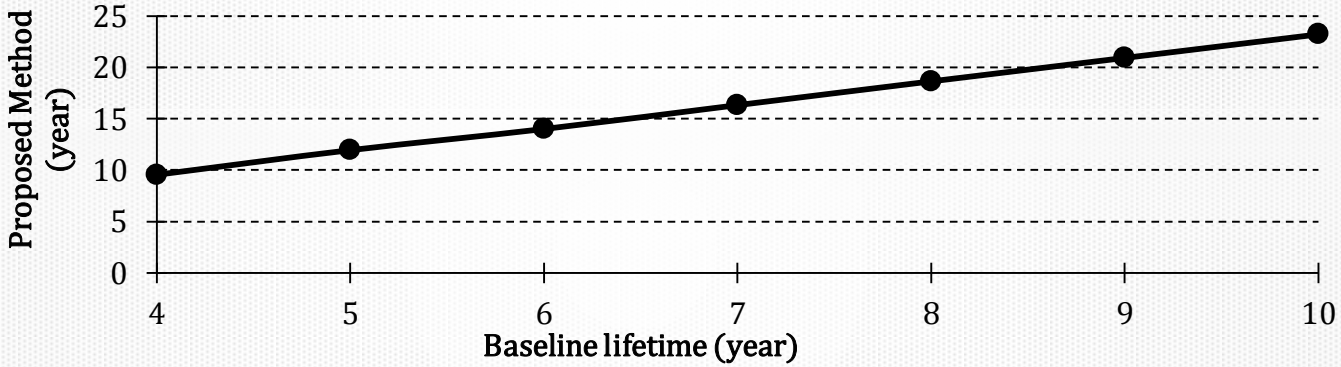


Results (cont.)

Performance Overhead



Lifetime Improvement



Future Work

- Generalization
  - Commercial FPGA Parameters
    - SB multiplexer
      - Size, pass gate vs. transmission, two-level versus tree-based
    - Wire length
    - Switch matrix topology
- Impact of Temperature Distribution, Process Variation, etc.
- Impact on Soft Error Rate

Questions

Thanks for Your Patience!