Session S4b

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# A Low-Power MTJ-Based Nonvolatile FPGA Using Self-Terminated Logic-In-Memory Structure

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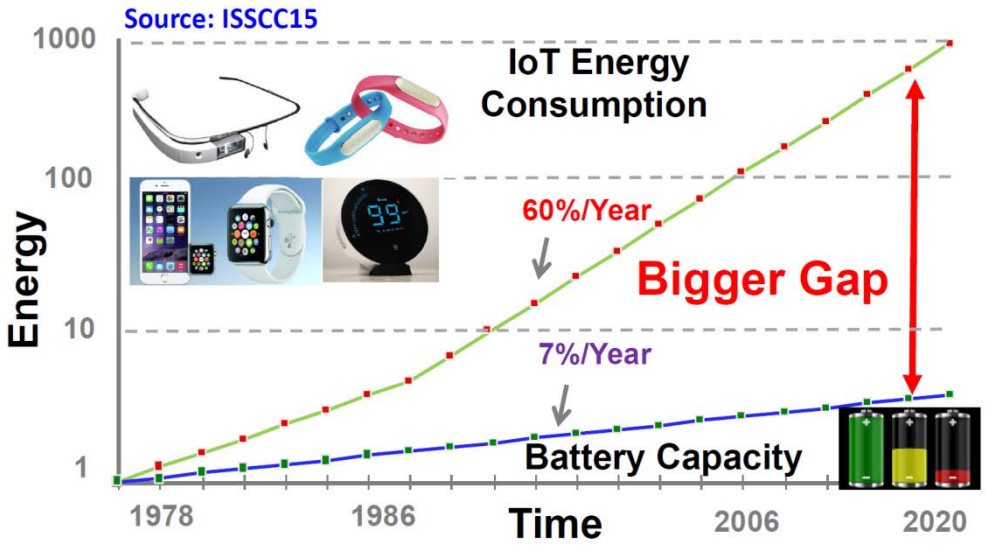
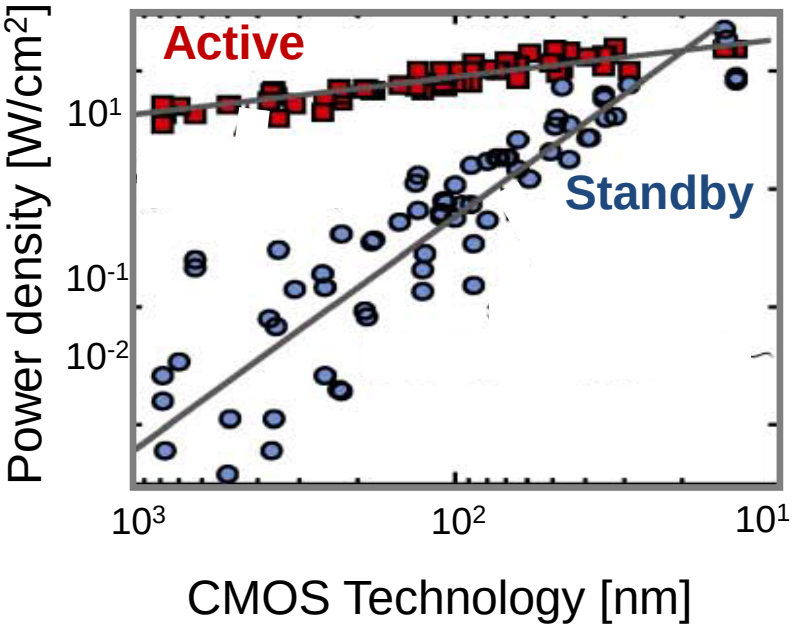
# Background

■ **FPGA (Field-Programmable Gate Array)**

→ Various digital systems are implemented with short design time and low cost.




[Ref.] Y. Liu, et al., ISSCC, pp. 84-85, Feb. 2016.




[Ref.] E. Pop, Nano Res. 3 (2010) 147.

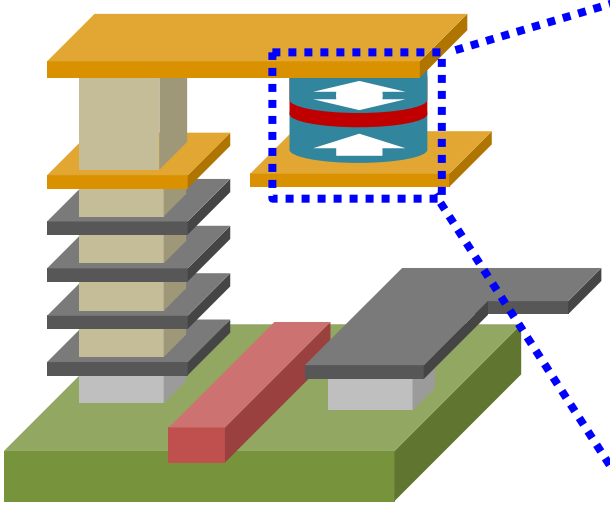
**A large number of HW components are embedded for reconfigurability**

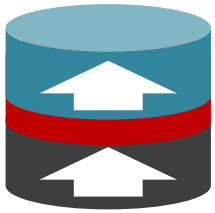
⇒ Low area & energy efficiency

Large amount of **standby power** due to nano-scale CMOS process

**How to overcome standby power problem of FPGA?**

# MTJ Device





$R_P$
(Low res.)

$R_{AP}$
(High res.)

- High endurance
- Scalability
- CMOS compatibility
- 3D-stacking

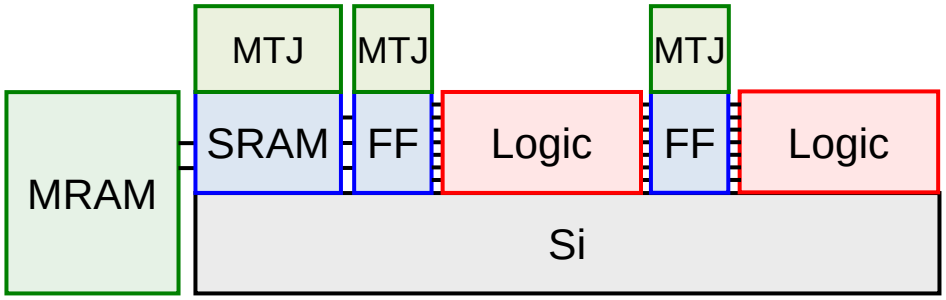
| Storage element | SRAM | ReRAM device | Atom switch | CAAC-IGZO | **MTJ device** |
|---|---|---|---|---|---|
| Nonvolatile | No | Yes | Yes | Yes | **Yes** |
| Scalability | + | ++ | ++ | -- | **++** |
| Endurance | ++ | - | -- | + | **++** |
| Write access | ++ | + | - | + | **++** |

**MTJ device is the best candidate for realizing nonvolatile logic.**

# MTJ-Based Nonvolatile Logic Families

## 1st Generation

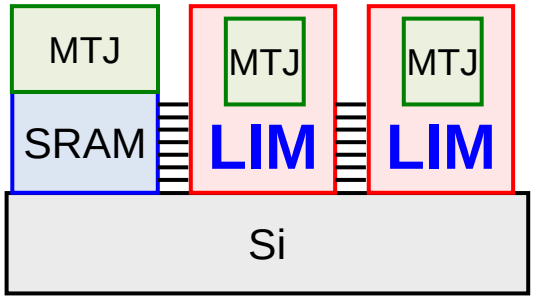
Storage elements are replaced by nonvolatile ones.



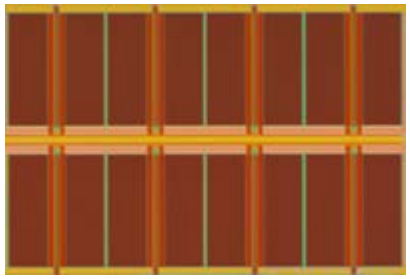

## 2nd Generation

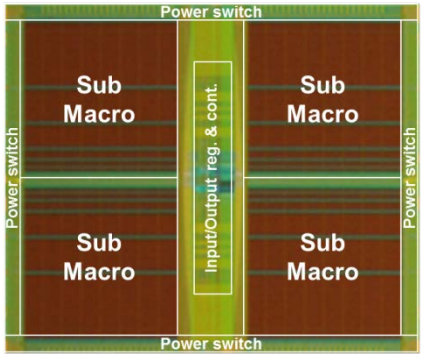
Storage and logic functions are merged.

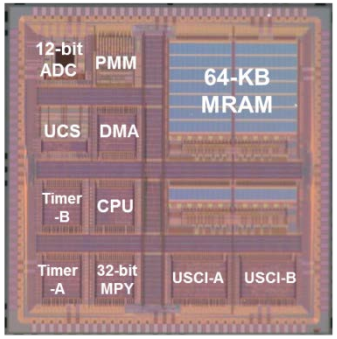
→ **Logic-in-memory (LIM) structure**

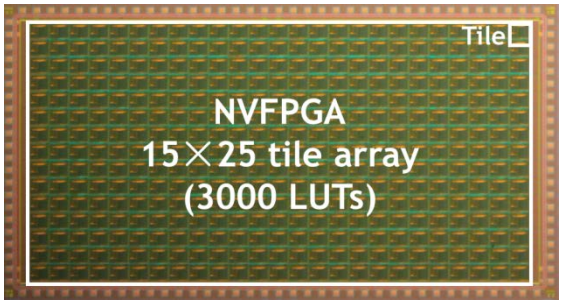



**JSPS FIRST program (Leader Prof. H. Ohno)**





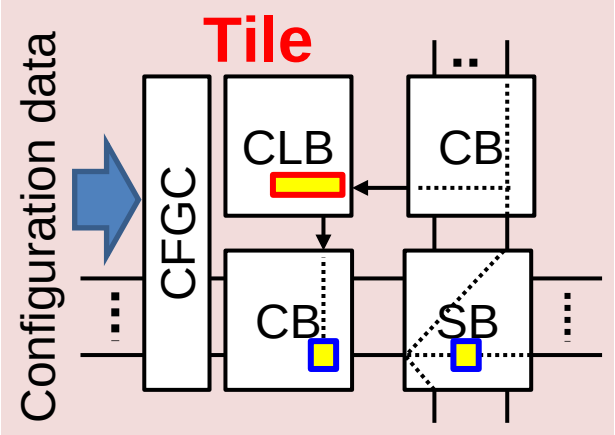



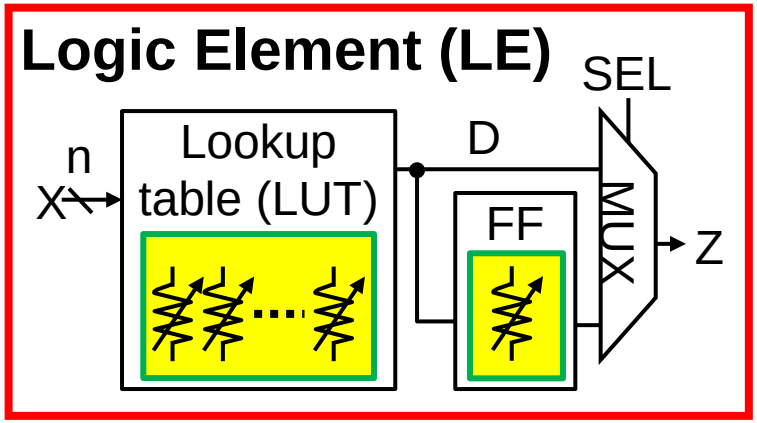



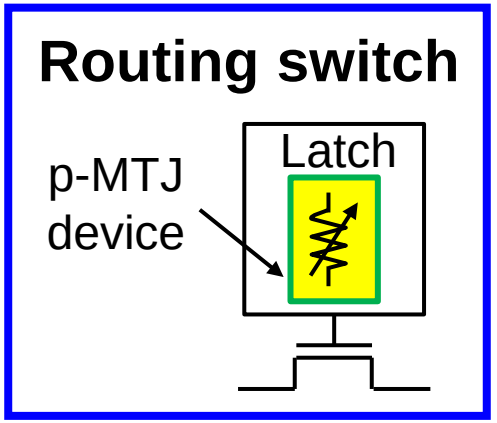

T. Ohsawa, et al., VLSIC, 2013. S. Matsunaga, et al., VLSIC, 2013. N. Sakimura, et al., ISSCC, 2014. D. Suzuki, et al., VLSIC, 2015.

**MTJ device is the best candidate for realizing Nonvolatile logic LSI.**

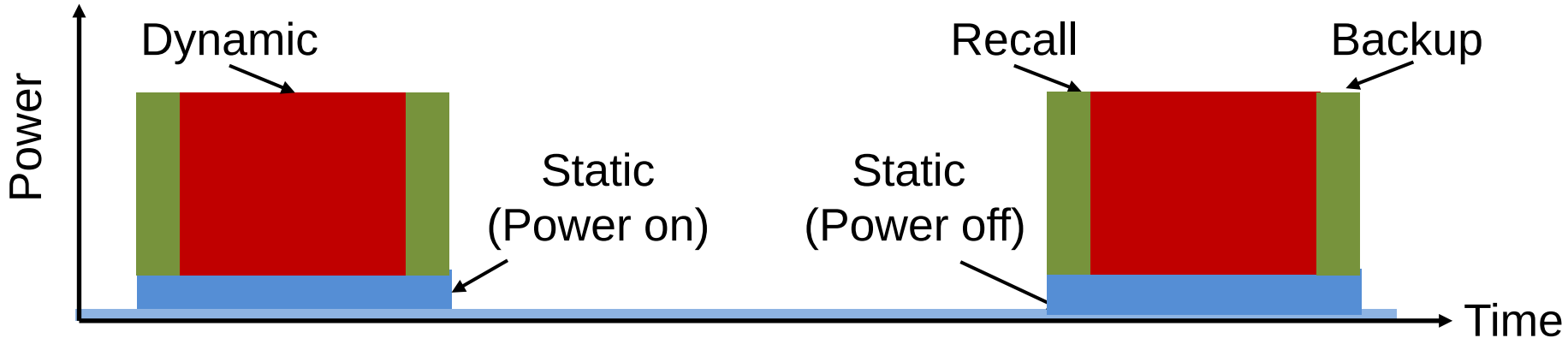
# Design Issue



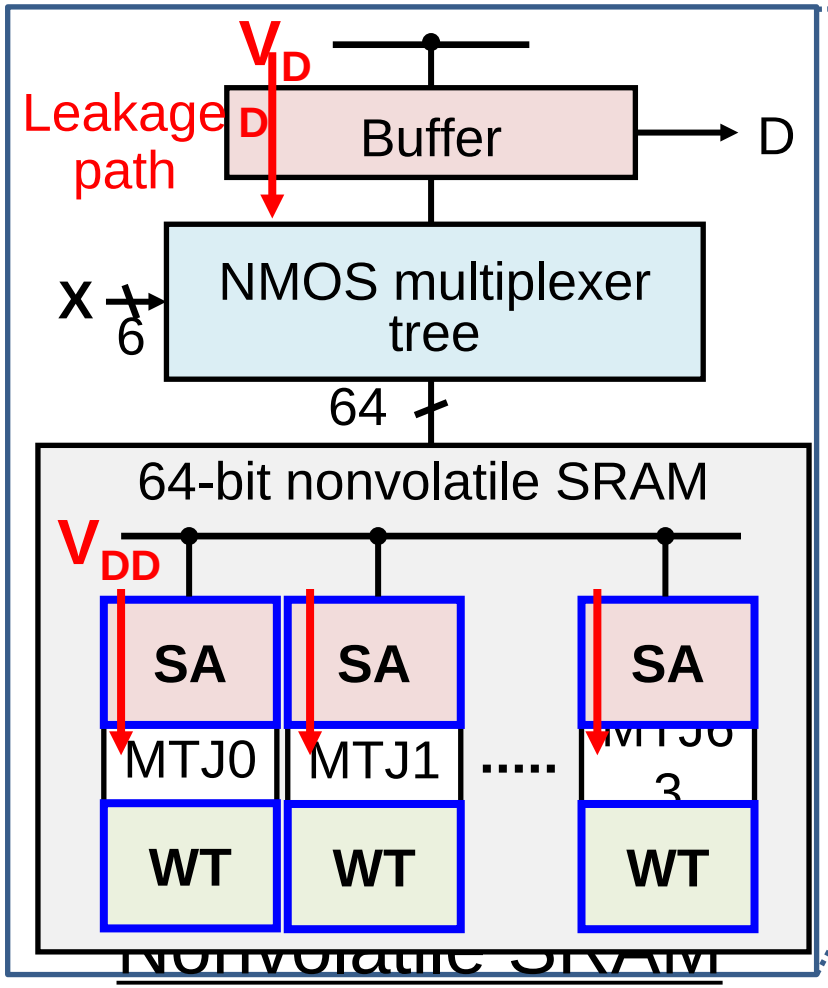




CLB: Configurable logic block CB: Connection block SB: Switch block CFGC: Configuration circuit

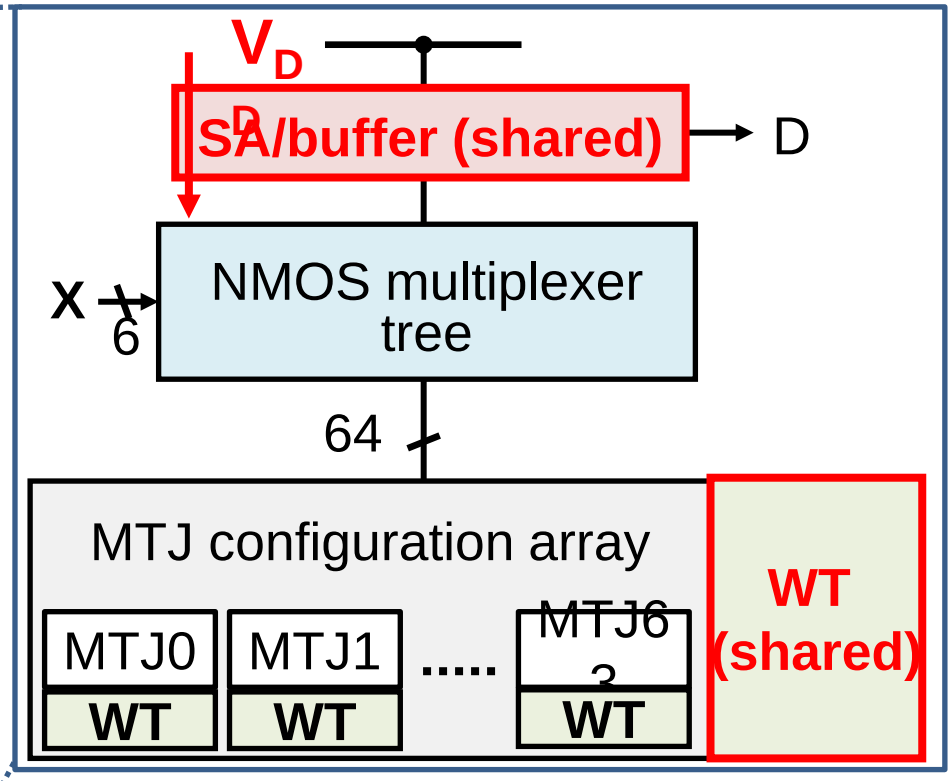



1. **Reduction of the overhead due to recall/backup operations**
2. **Reduction of the number of leakage current paths**

# Logic-In-Memory Structure




Nonvolatile SRAM based



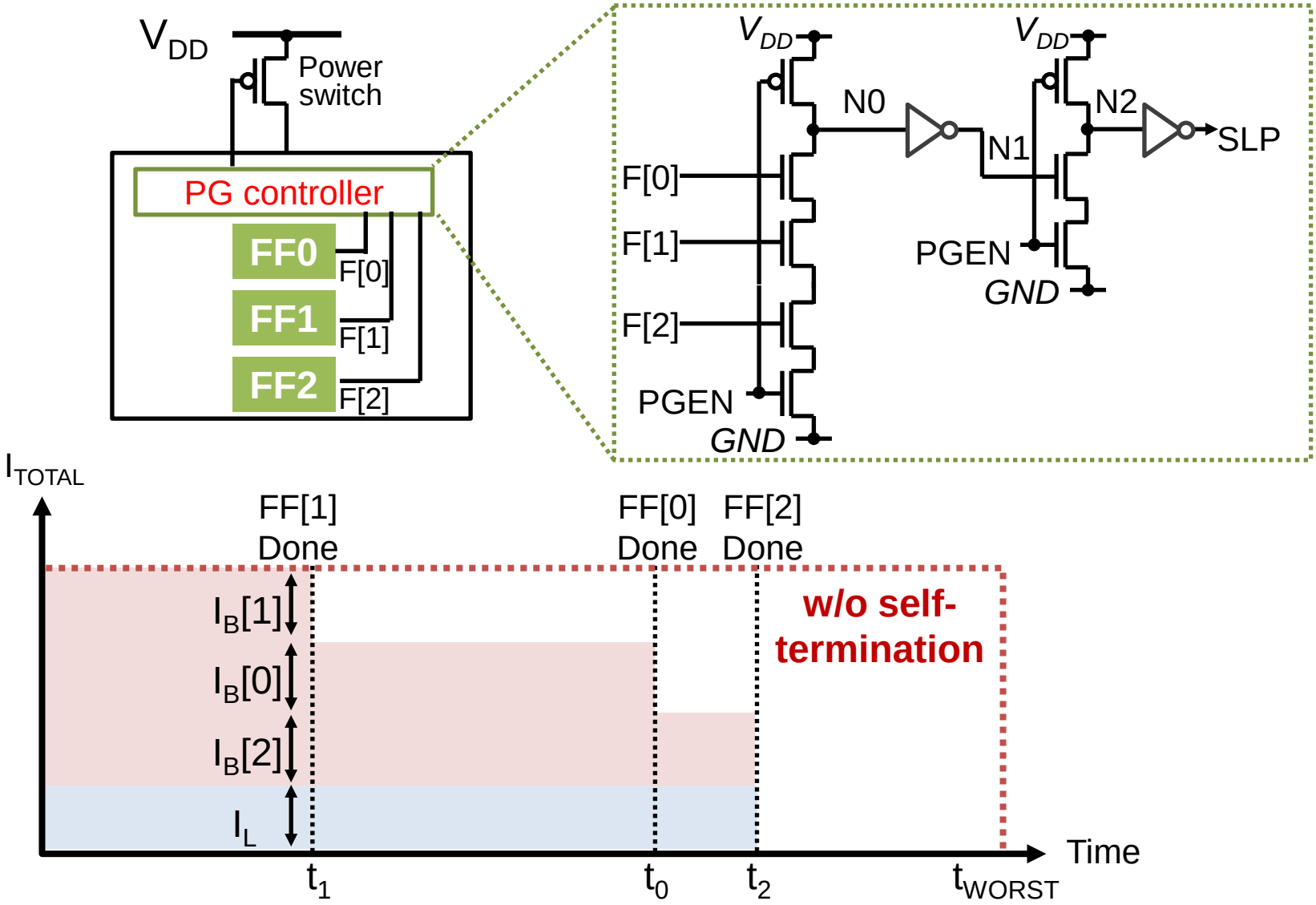

SA: Sense amplifier WT: Write transistor

Both SAs and WDs are shared.

**Proposed**

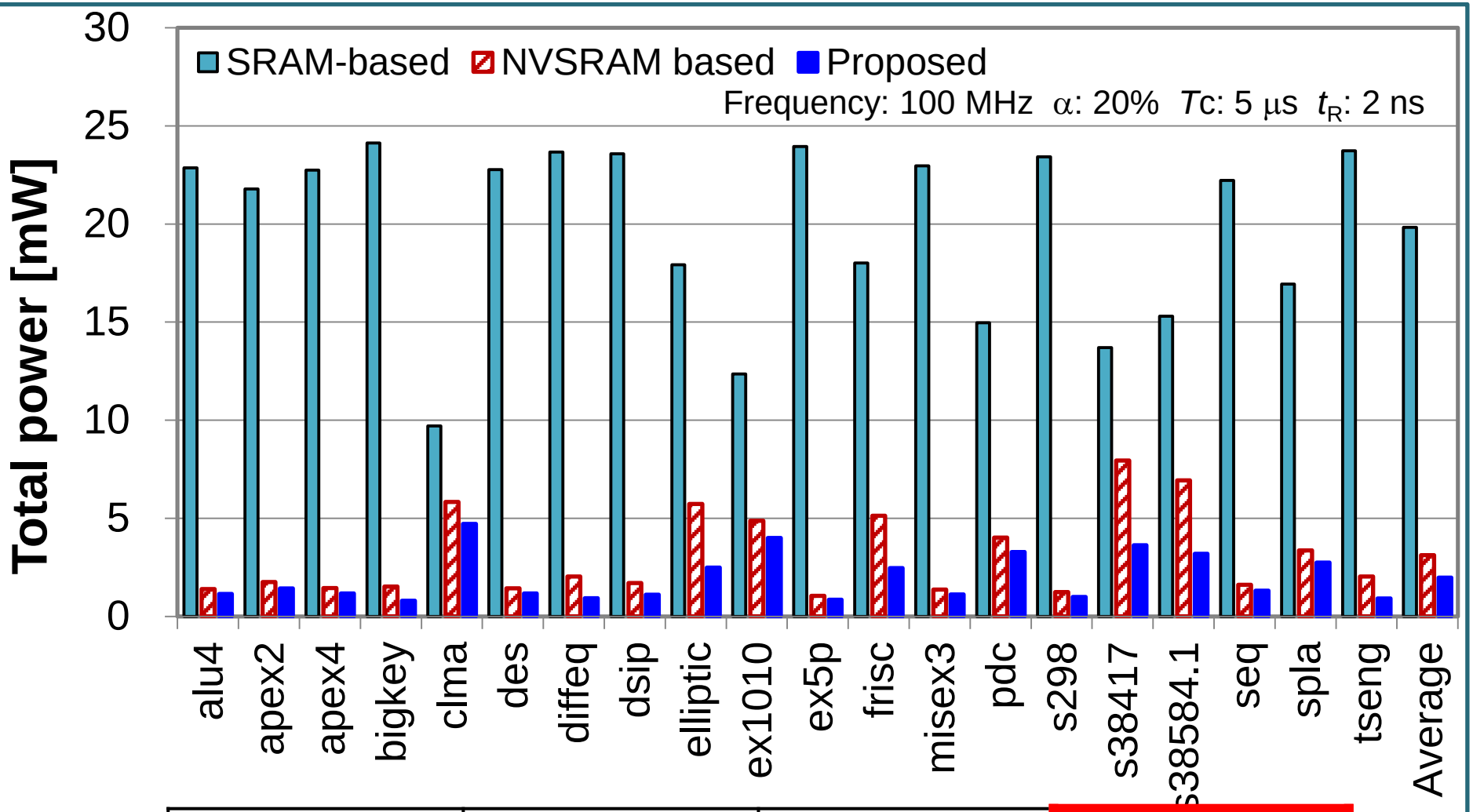
**Compact circuitry with small number of leakage current paths**

# Self-Terminated Power-Gating Scheme




Minimization of both backup energy and leakage energy.

# Evaluation




| | SRAM-based | NVSRAM based | **Proposed** |
|---|---|---|---|
| Average total power | 19.8mW | 3.12 mW | **1.97 mW** |

# Thank you!