Resource Efficient Real-Time Processing of Contrast Limited Adaptive Histogram Equalization

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Outline

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- Histogram Equalization
  - General Histogram Equalization
  - Adaptive Histogram Equalization
  - Contrast Limited Adaptive Histogram Equalization
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- Contextual CLAHE
  - Histogram Generation
  - Histogram Distribution and CDF
  - Interpolation Technique
- Testbed
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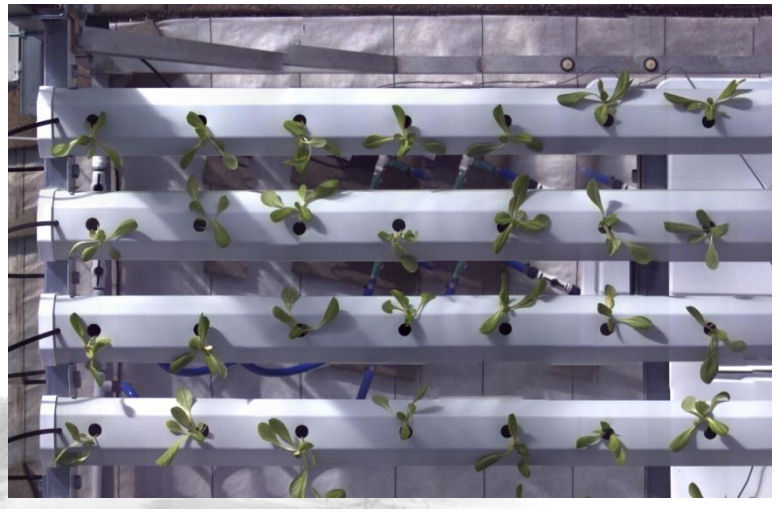
- Conclusion and Future Work

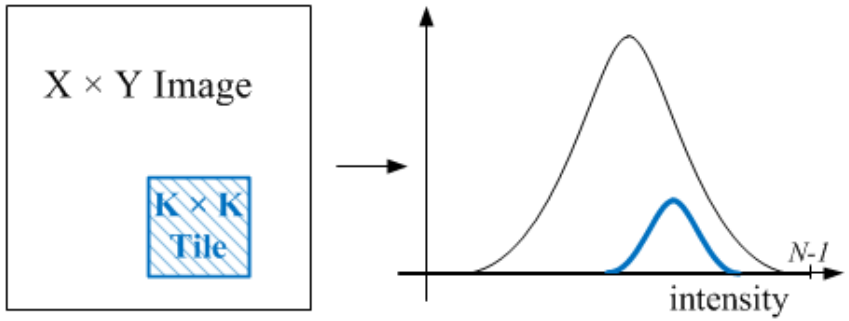
Motivation

- Contact Sensing
  - Burdensome
  - Labor-intensive
  - Destructive
- Non-contact Sensing
  - Structural challenge
  - Sunlight variety
  - Poor image quality

How can we enhance the image quality ?

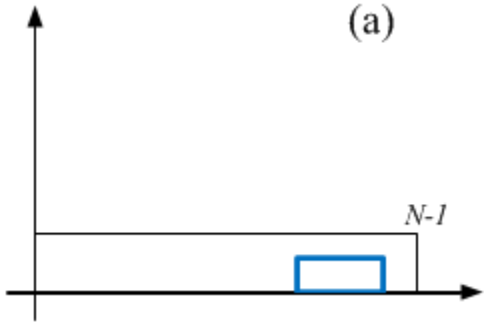


Histogram Equalization

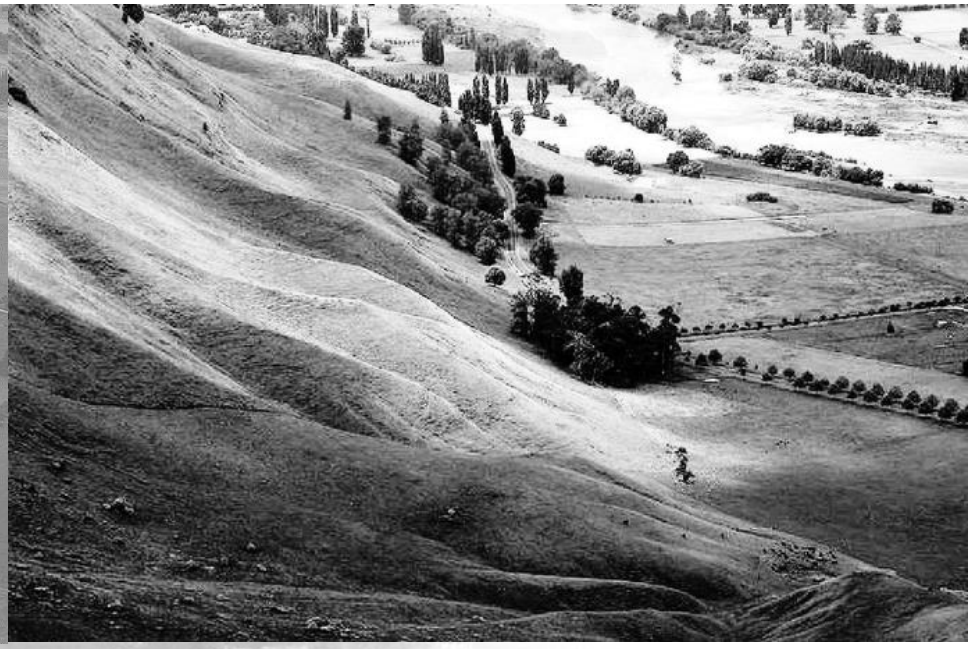


Input Image

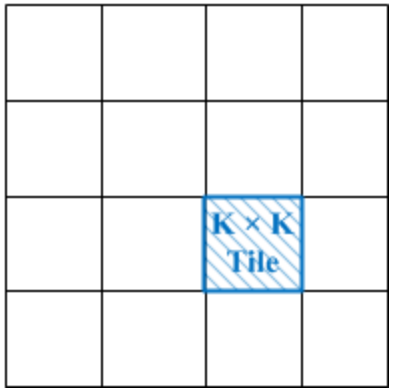
Image Histogram



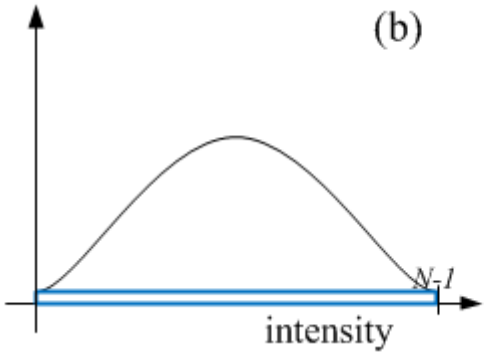
(a) Histogram Equalization (HE)



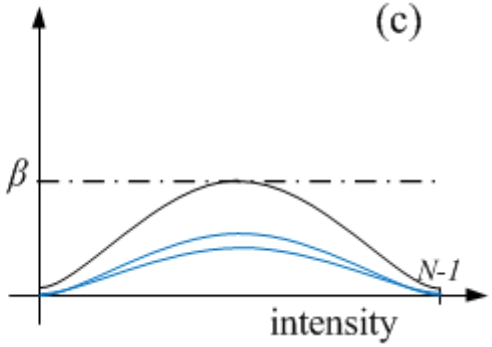
Adaptive Histogram Equalization



Input Image

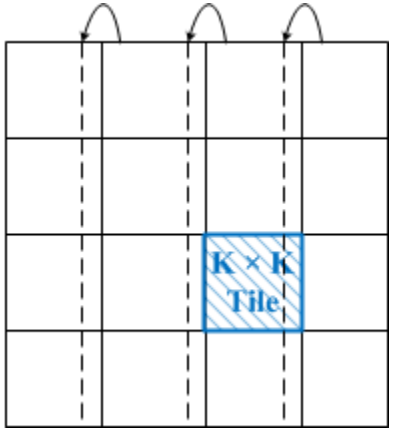


(b) Adaptive HE (AHE)

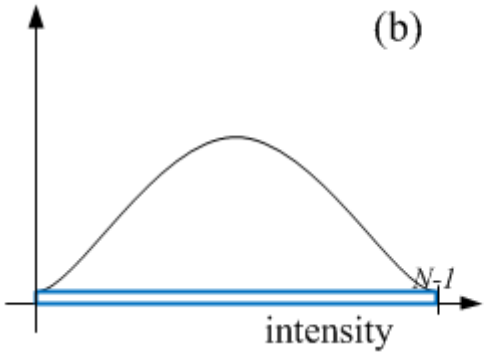


(c) Contrast Limited AHE (CLAHE)

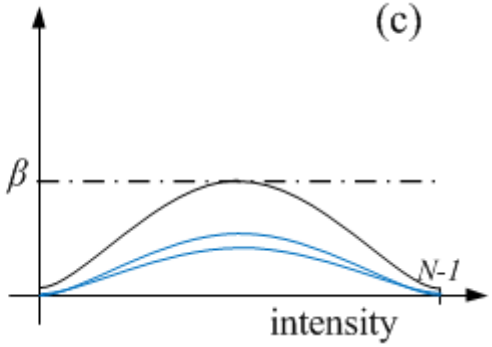
Adaptive Histogram Equalization



Input Image

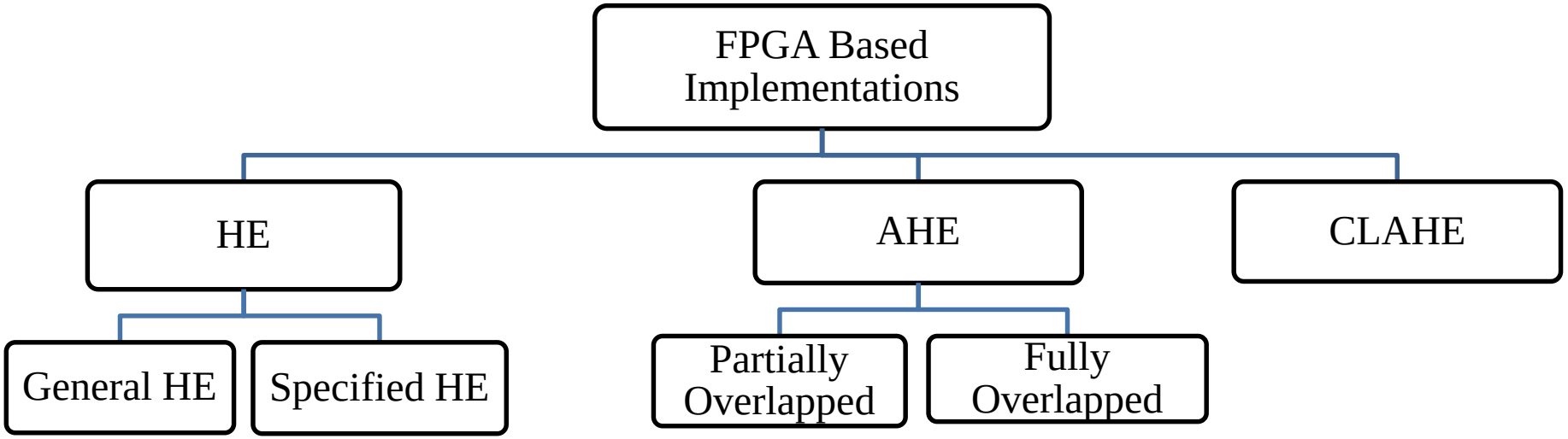


(b) Adaptive HE (AHE)



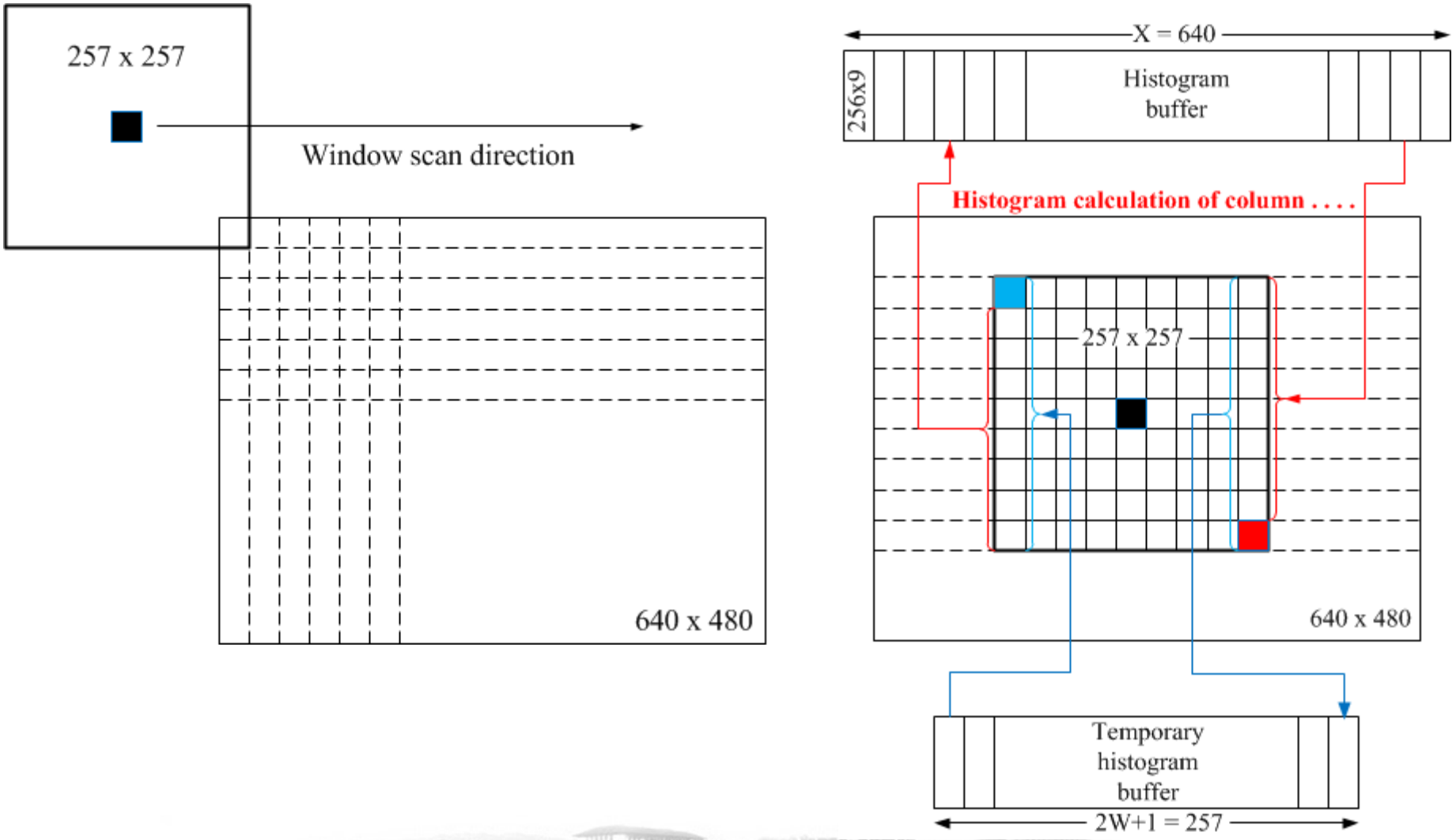
(c) Contrast Limited AHE (CLAHE)

Related Works

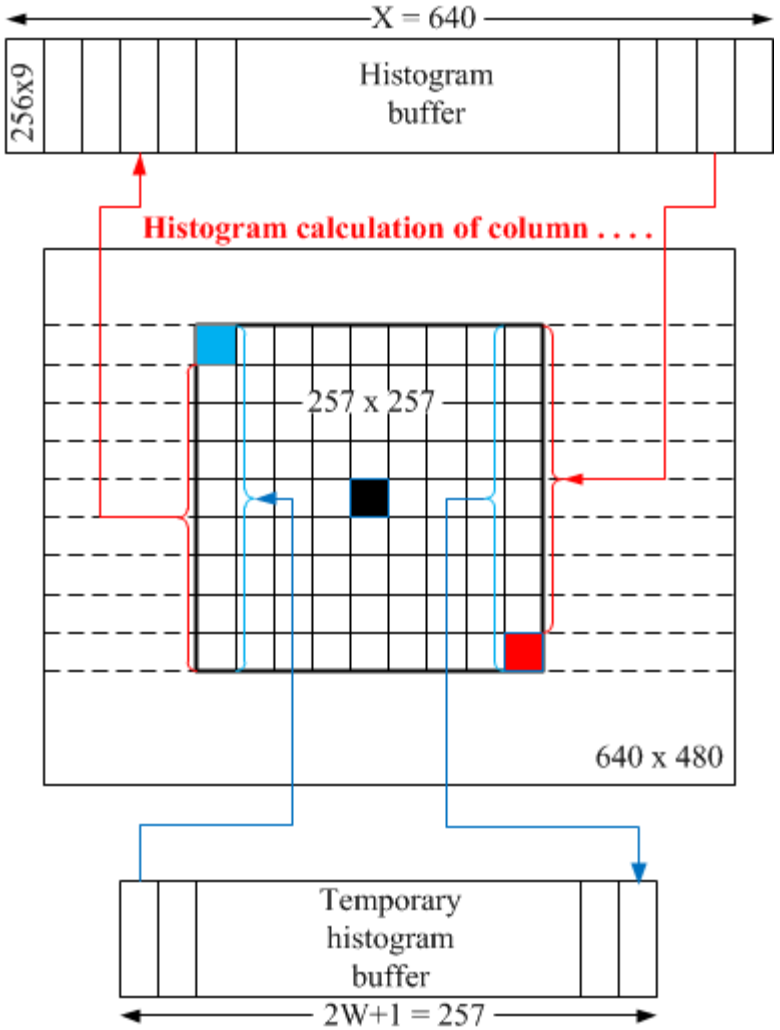


HE	Specified HE	Specified HE 2	AHE	CLAHE
- 720 × 480 - 122 fps - Missing local details	- 128 × 128 - 25 fps - For specific task	- 2.5Mpixels - 25 fps - For specific task	- 640 ×480 - 263.8 fps - 128 block RAMs	- 640x480 - 537.9 fps - Extremely memory depended (192 BRAM)

Existing CLAHE Implementation



Existing CLAHE Implementation



Pros:

- Real-time implementation
- 537.9fps
- The speed of algorithm is independent from image size

Cons:

- Requires 192x18K BRAM
- Larger image size needs 320 BRAM (1920x1080)
- Consume large amount of logic resource

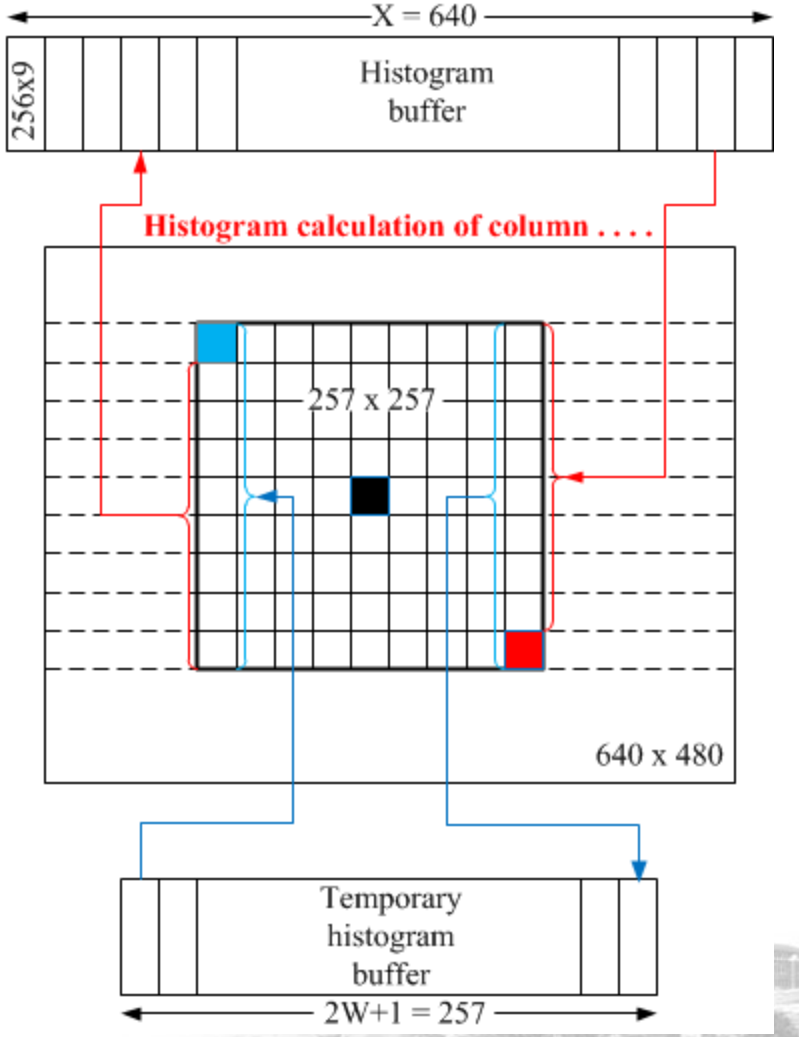
Contextual CLAHE

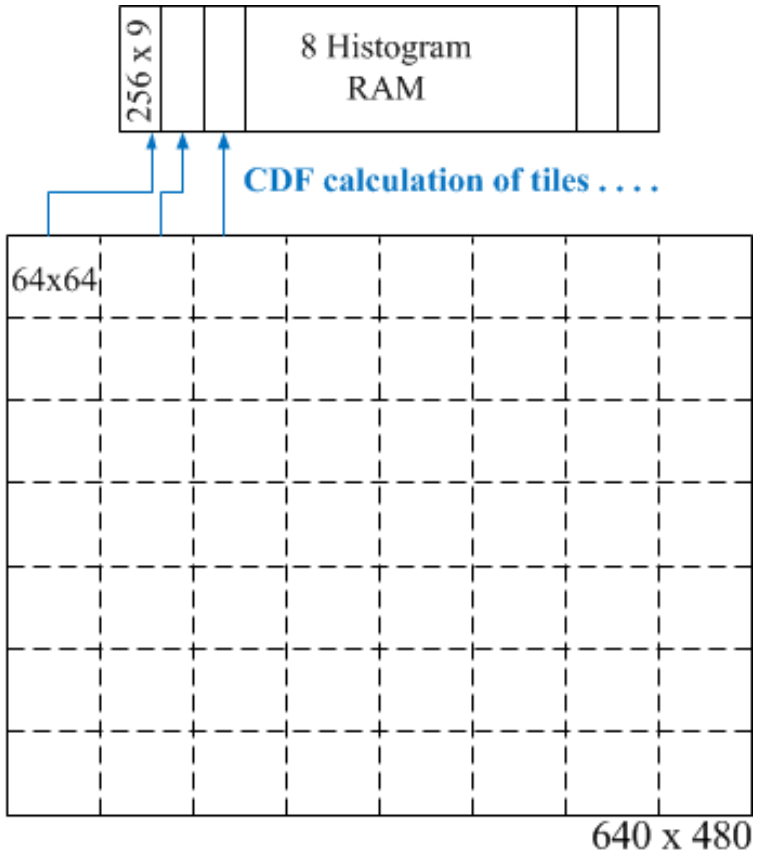
256 x 9 x 640 = 184.320 KB (HB)

256 x 9 x 257 = 70.016K KB (THB)

256 x 13 x 8 = 26.624 KB

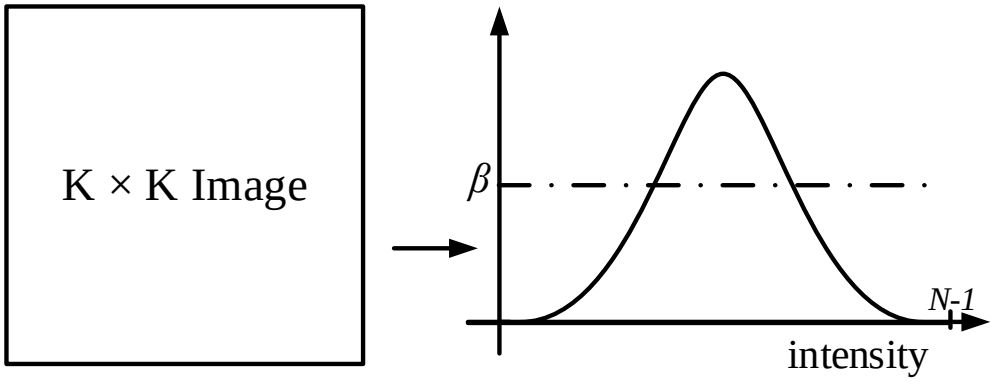
4 row = 106.496 KB



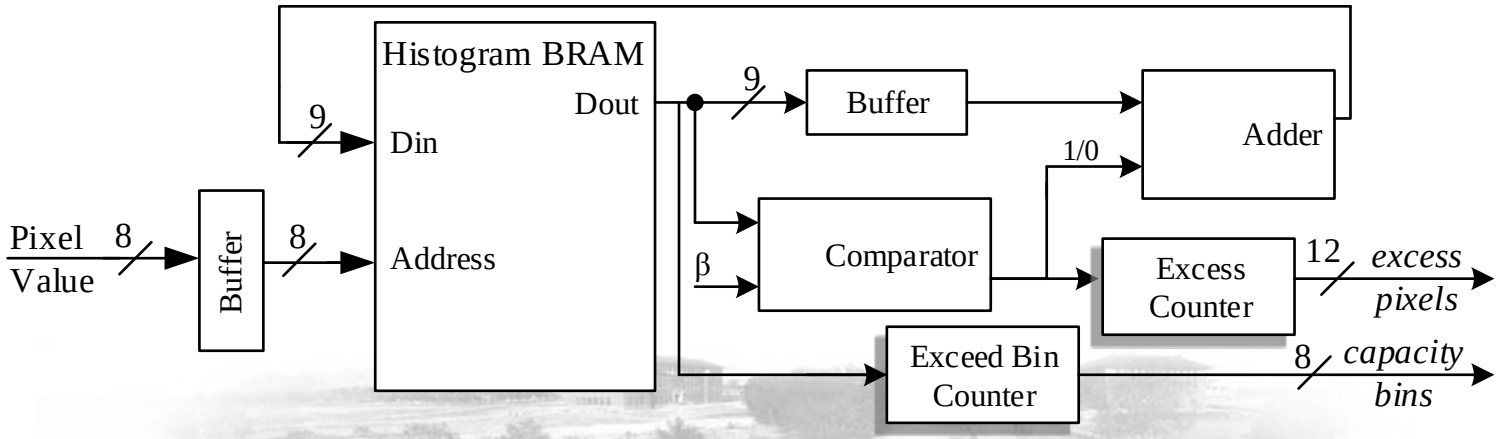


Combine tiles via interpolation.

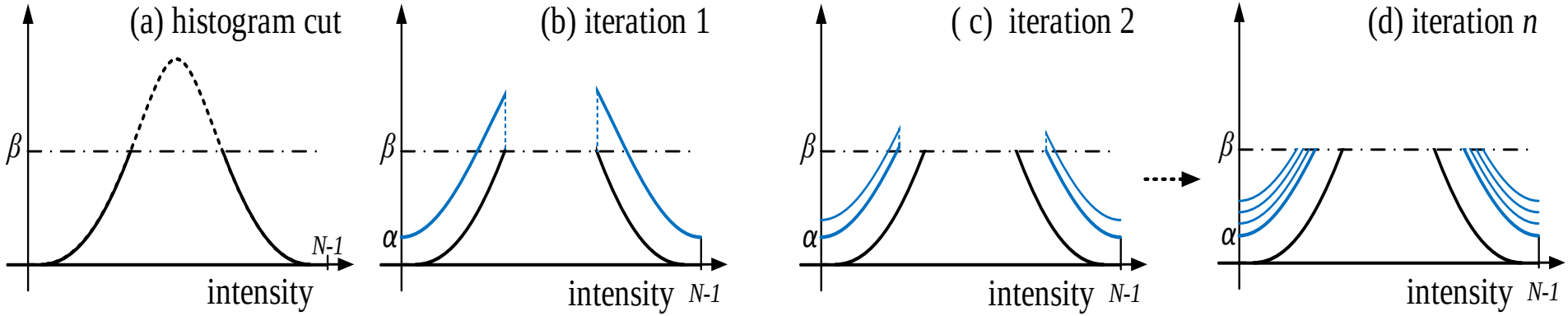
Histogram Generation



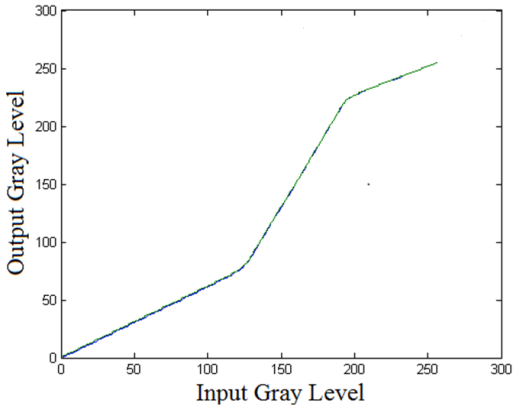
$$h(k) = \sum_{k=0}^{255} \begin{cases} 1, & I(i) = k \\ 0 & other \end{cases} \quad (1)$$



Histogram Distribution & CDF

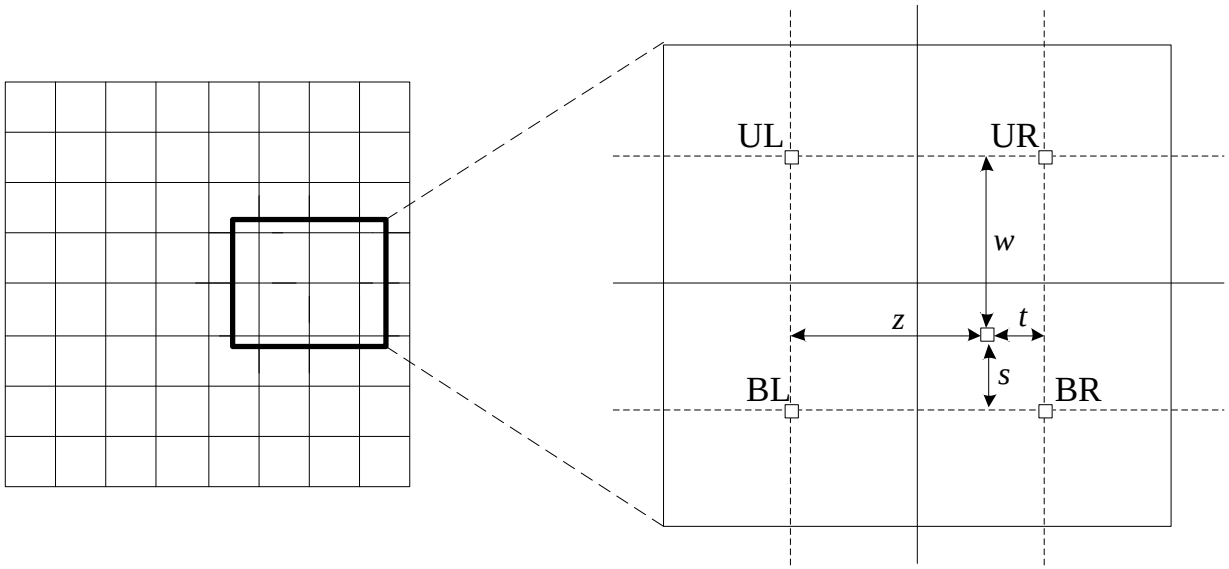


(e) CDF



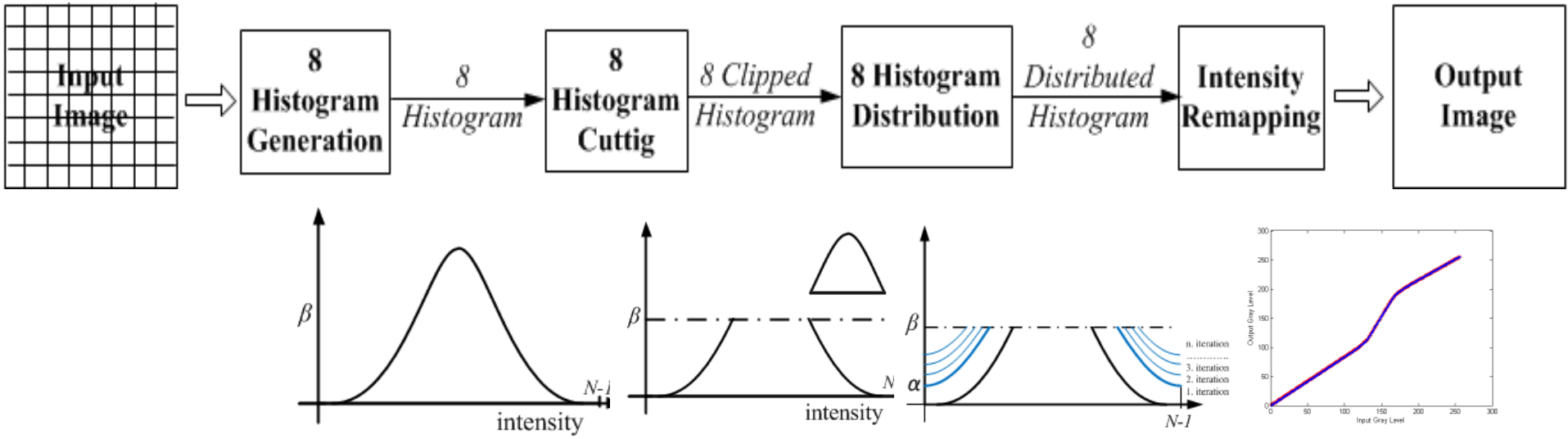
$$CDF = m_{x,y}(n) = \sum_{k=0}^{n} h(k) \times \frac{1}{M} \times N \qquad (2)$$

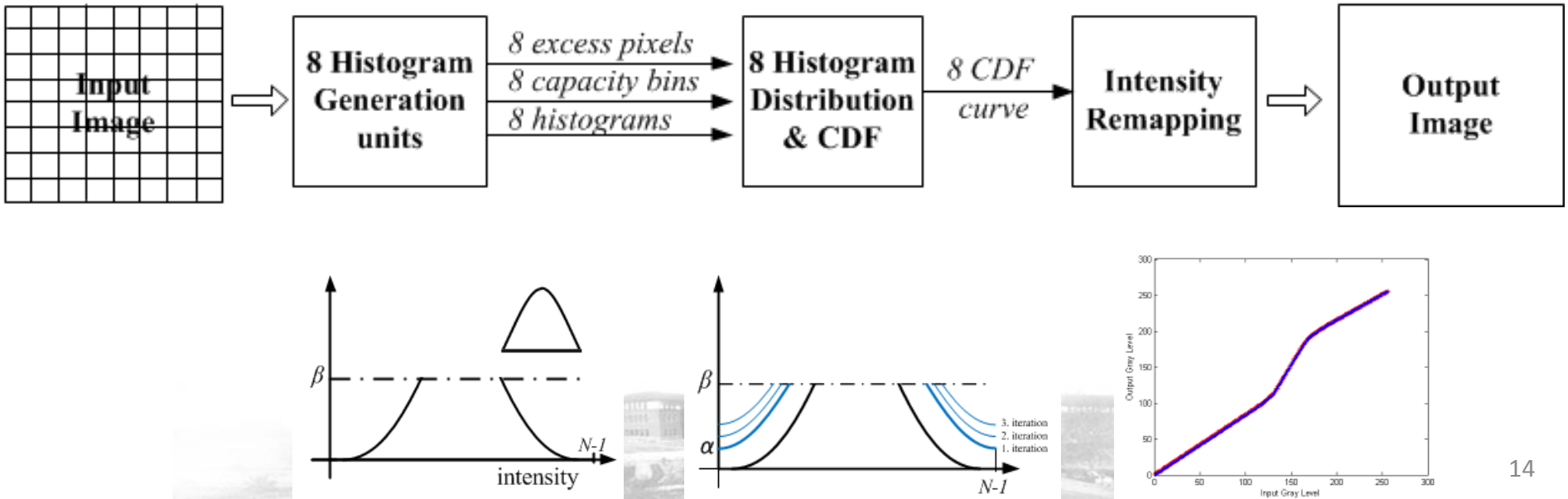
Interpolation Technique



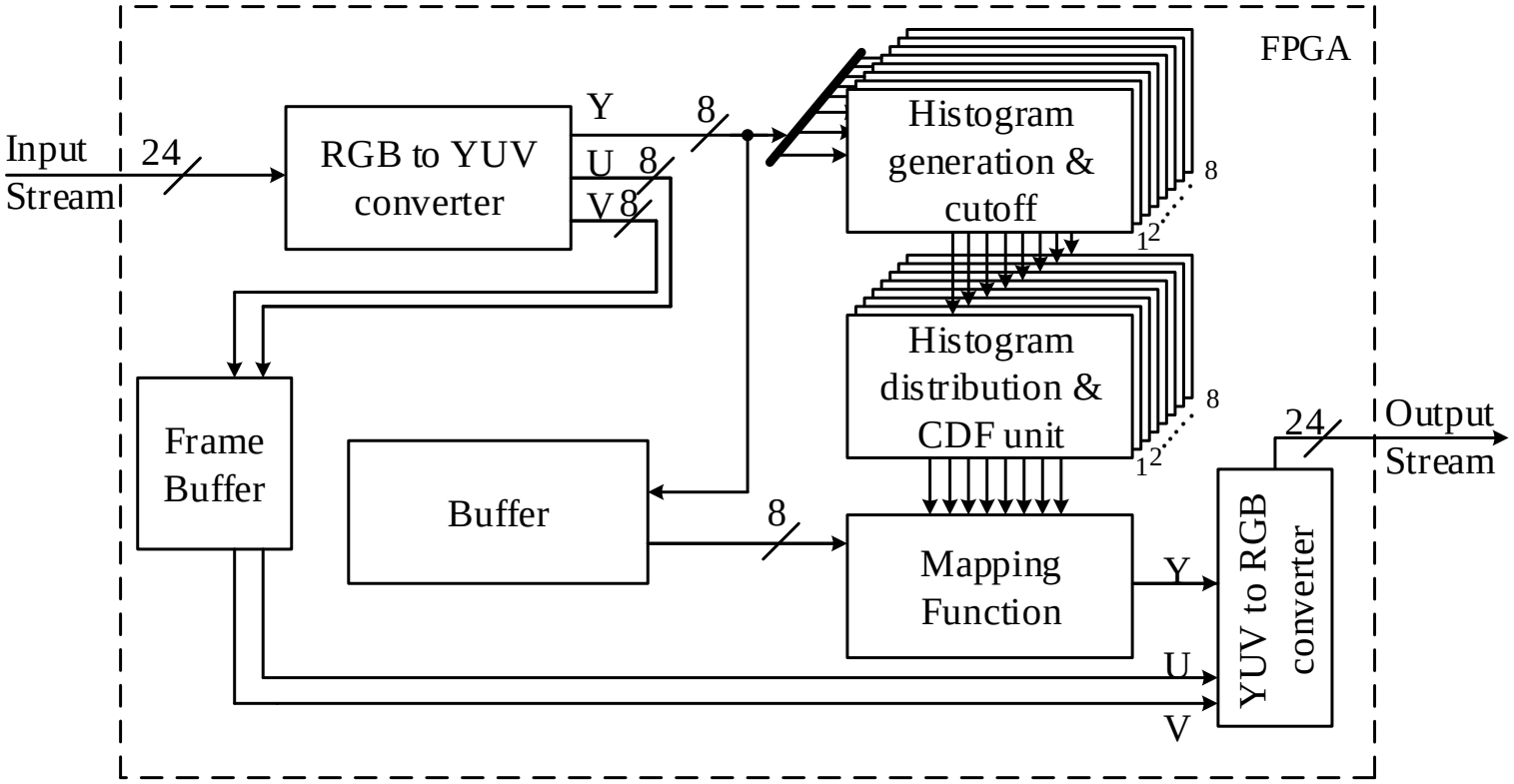
$$I_{new} = \frac{s}{s+w}\left(\frac{t}{z+t}m_{UL}(n) + \frac{z}{z+t}m_{UR}(n)\right) + \frac{w}{s+w}\left(\frac{t}{z+t}m_{BL}(n) + \frac{z}{z+t}m_{BR}(n)\right) \quad (3)$$

Contextual CLAHE



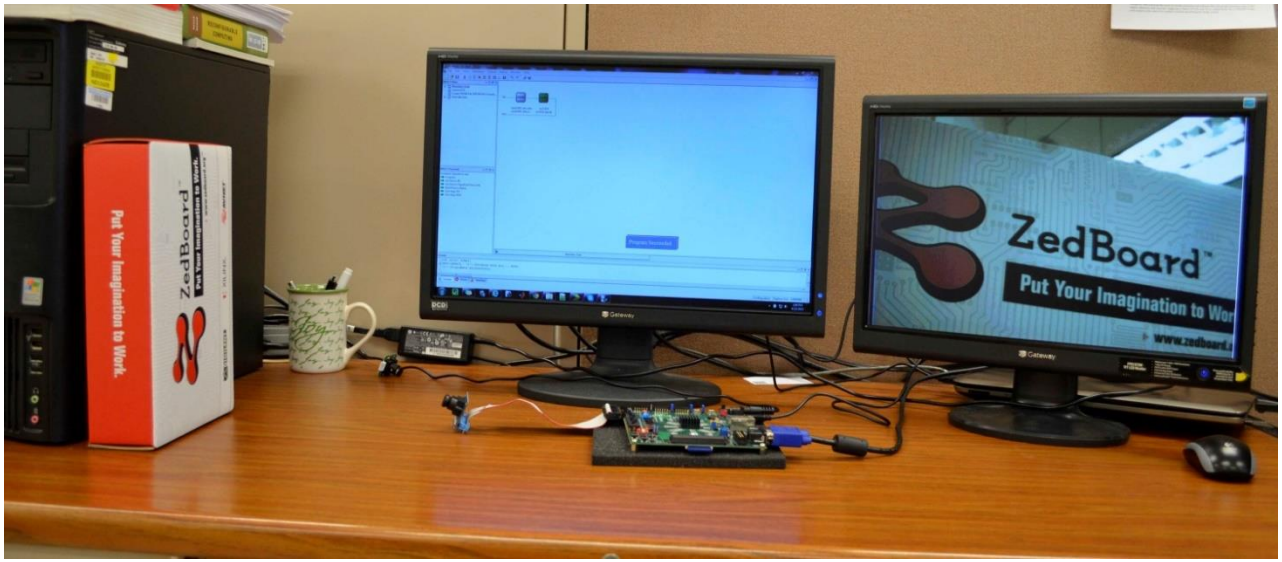


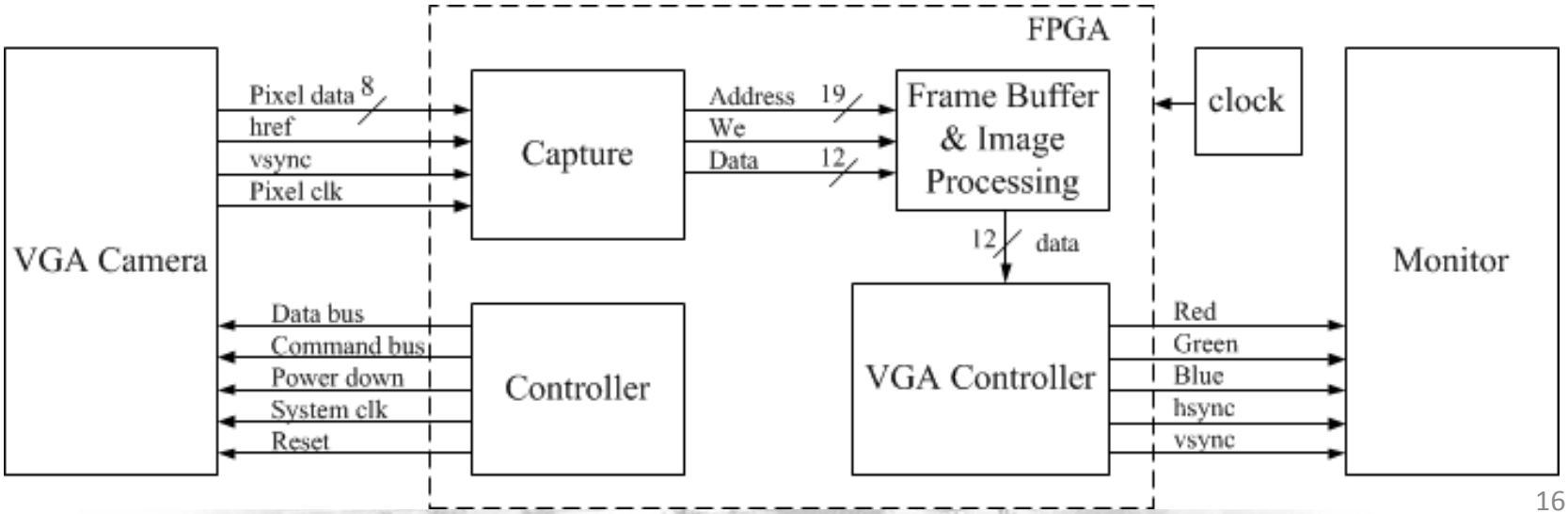
HE for Color Image



Y stands for the luma (the brightness).
U and V are the chrominance (color) components.

Testbed


ZedBoard
Put Your Imagination to Work.
ZedBoard
Put Your Imagination to Wor


FPGA
VGA Camera
Pixel data
8
href
vsync
Pixel clk
Capture
Address
19
We
Data
12
Frame Buffer & Image Processing
clock
Monitor
12
data
Data bus
Command bus
Power down
System clk
Reset
Controller
VGA Controller
Red
Green
Blue
hsync
vsync

Histogram Equalization Results

(a) Original Image

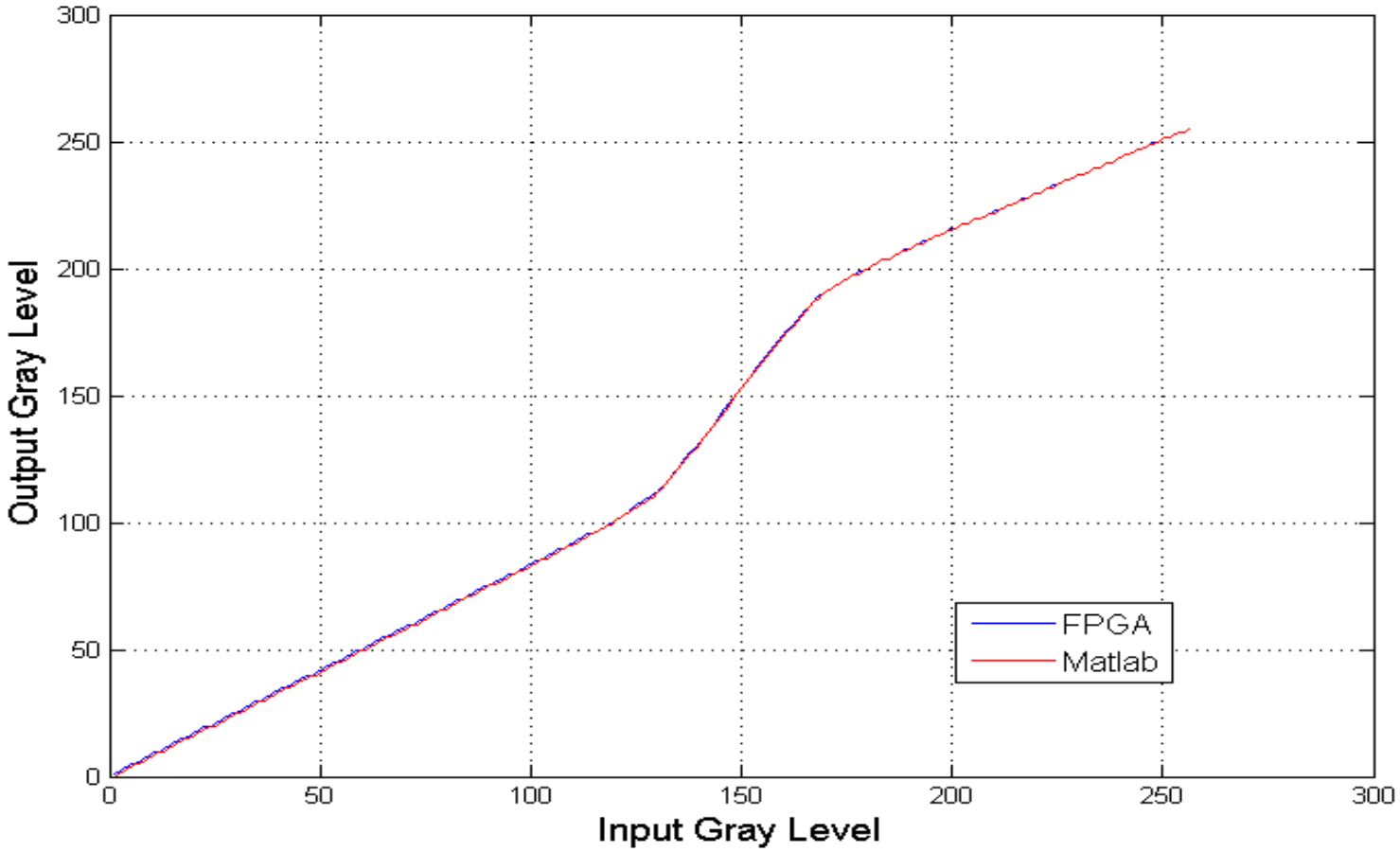
(b) Enhanced Image

Histogram Equalization Results

(a) FPGA

(b) Matlab

Histogram Equalization Results



FPGA and Matlab based output comparison with 0.39% difference

$$\text{error rate} = \frac{1}{250}$$

Histogram Equalization Results

Logic Resource	CCLAHE	CLAHE
Number of Slice Registers	440	246
Number of Slice LUTs	4766	32123
Number of fully used LUT-FF pairs	284	222
Number of Block RAM/FIFO	16	192
Operatinal Frequency	108.86 MHz	209.6 MHz
Performance	354.36 fps	537.9 fps

	Frame Size			
	512 x 512	640 x 480	1280 x 720	1920 x 1080
Critical Path Delay	8.475 ns	9.186 ns	12.061 ns	14.479 ns
Maximum Operational Frequency	117.99 MHZ	108.86 MHz	82.91 MHz	69.06 MHz
Performance	450.111 fps	354.36 fps	89.96 fps	33.30 fps

Conclusion and Future Work

- Real-time processing of CLAHE.
- First implementation of interpolation based Contextual CLAHE.
- Introduced a method for real time implementation of Contextual CLAHE to solve memory dependency issue.
- Modified the flow of algorithm for FPGA implementation.
  - Histogram generation method is restructured to reduce block RAM usage.
  - Histogram redistribution technique is proposed to implement iterative redistribution algorithm in hardware.
- Alternative interpolation calculation method is proposed to the computation complexity.

- Histogram equalization architecture will be parallelized to increase its performance for larger image size.
- Investigate different transfer function for calculating CDF.
- Contrast-sensitive transfer function.

Q & A