Efficient Sum of Absolute Difference Computation on FPGAs

International Conference on
Field Programmable Logic and Application (FPL)
2016

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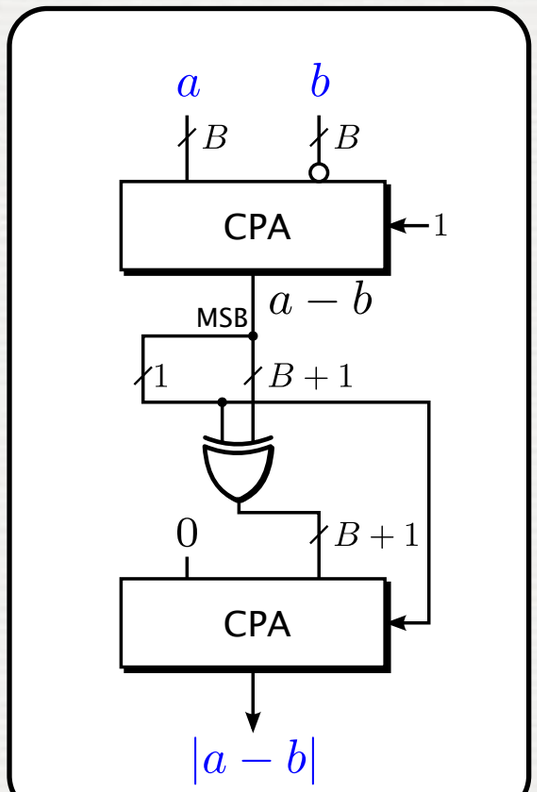
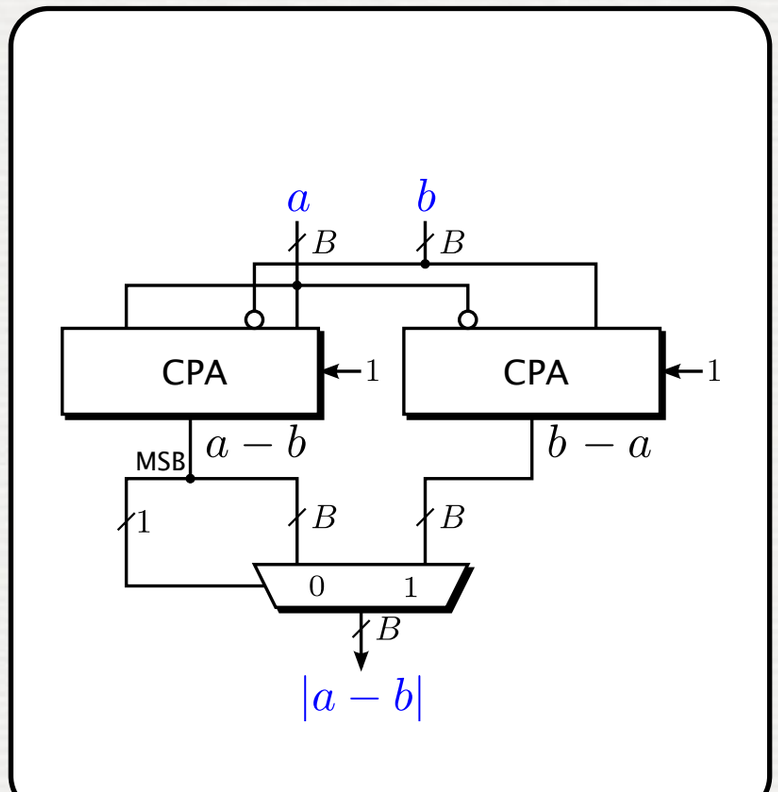
Sum of Absolute Difference (SAD)

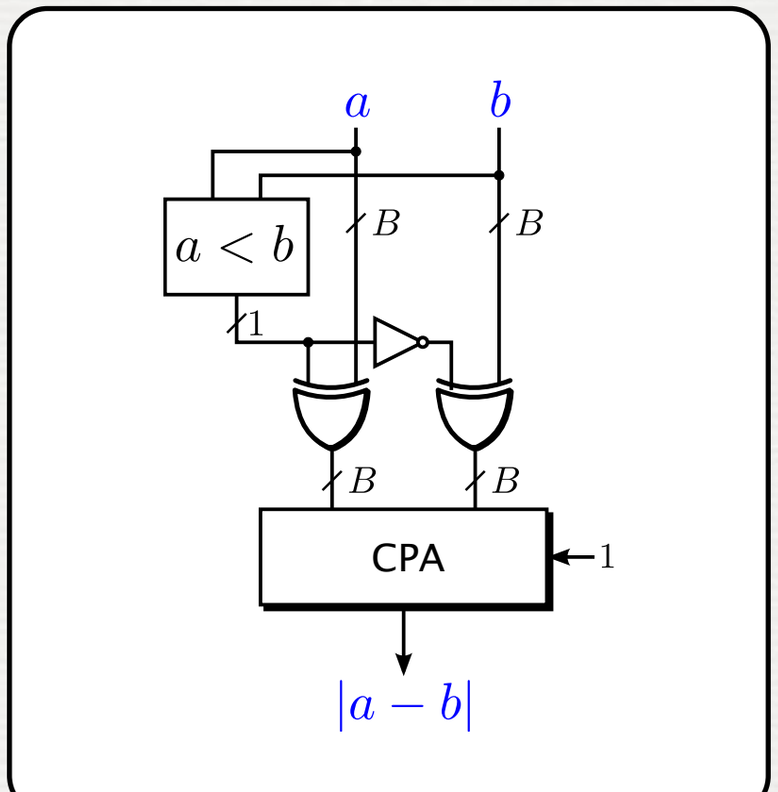
- SAD is an important operation in image and video processing
- Metric to measure the distance between two blocks of an image
- Applications are, e.g., *motion estimation* or *stereo matching*
- An $R \times C$ SAD operation of two matrices $\mathbf{A}$ and $\mathbf{B}$ is defined as:

$$\mathrm{SAD}(\mathbf{A},\mathbf{B}) = \sum_{i=1}^{R}\sum_{j=1}^{C} |a_{i,j} - b_{i,j}|$$

Previous Work



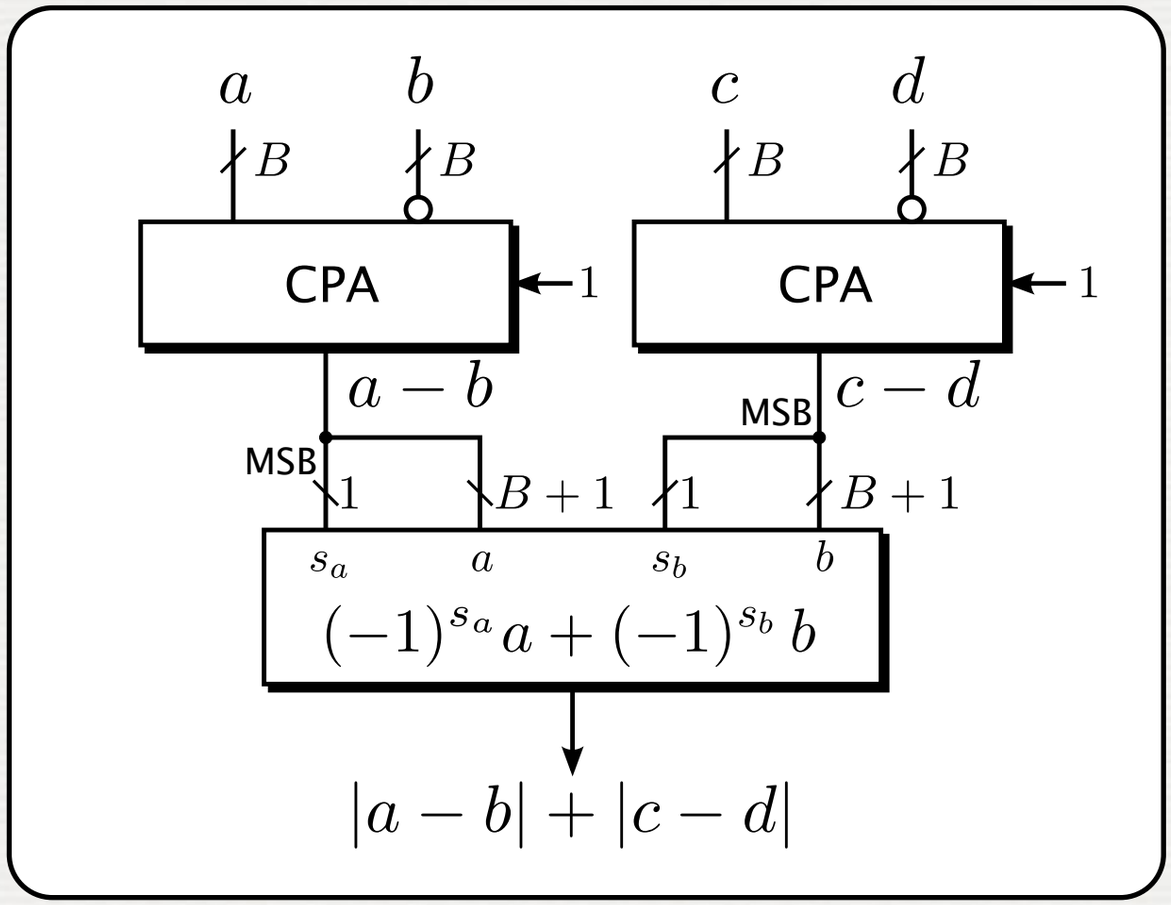




Sequential AD [1] **Parallel AD [2]** **FPGA optimized [3]**

- SAD is computed with N absolute difference (AD) units
- N-input adder tree / compressor tree required
- LUTs of best reported circuit grow with $2.5NB$ (B: word size)

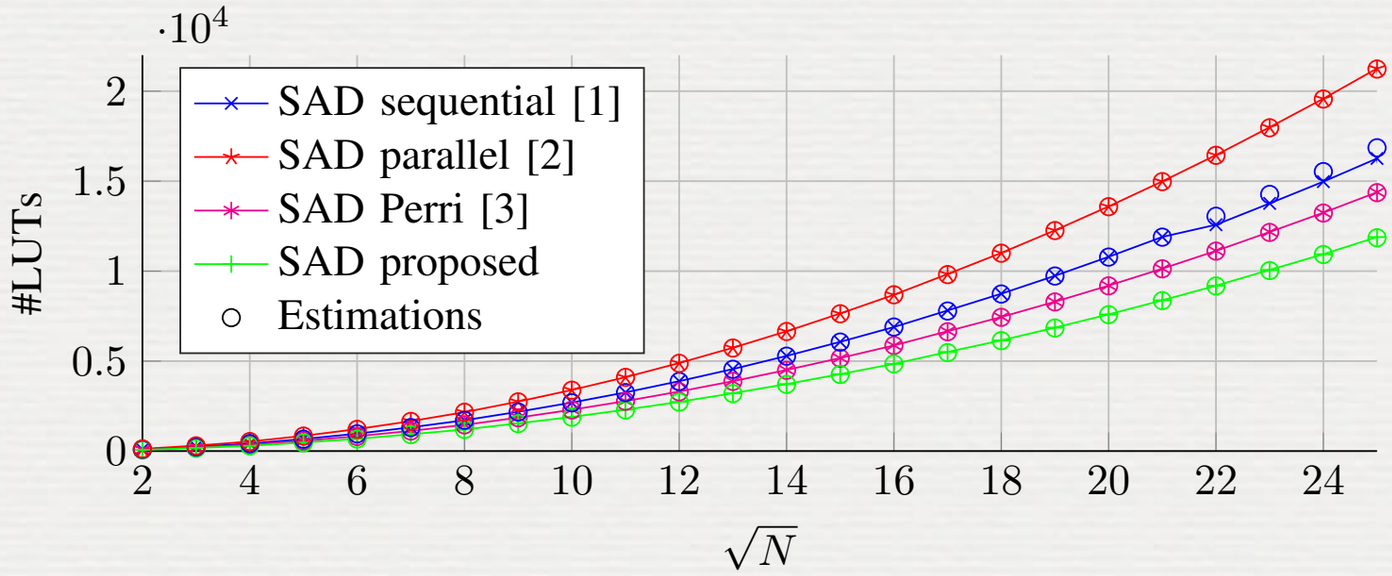
Proposed SAD



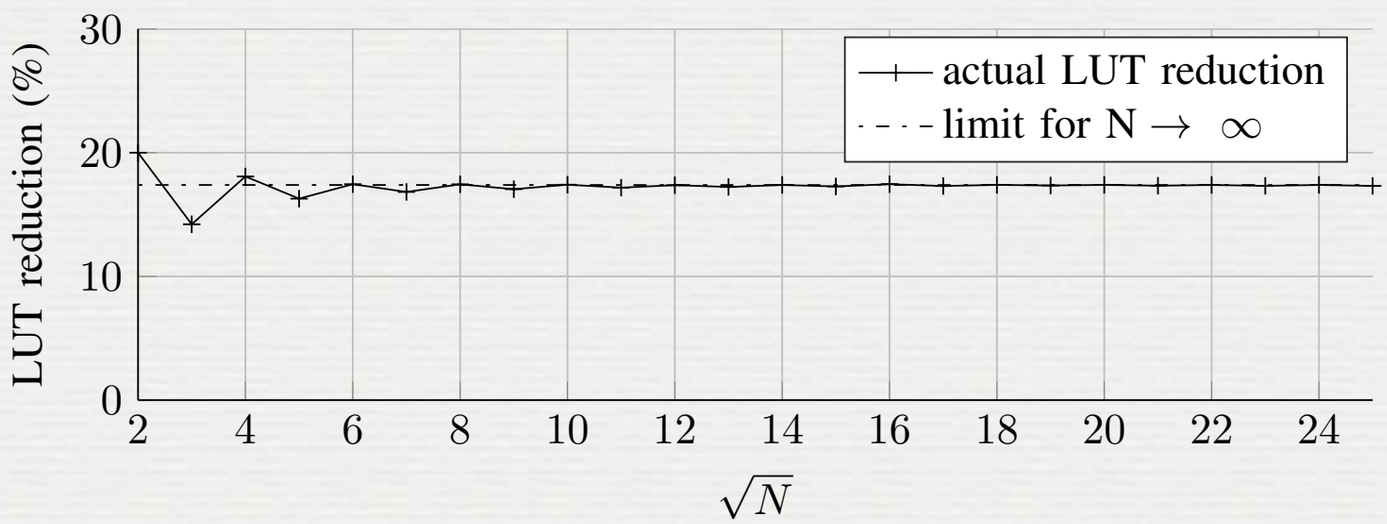
Proposed 1×2 SAD

- SAD is computed with $N/2$ 1x2 SAD units
- $N/2$-input adder tree / compressor tree required
- LUTs of proposed SAD grow with $2.0NB$ (B: word size)

Results



(a) Required and estimated LUTs



(b) Relative LUT reduction compared to [3]

Check out *uni_ks* git branch of

https://scm.gforge.inria.fr/anonscm/git/flopoco/flopoco.git

See you at the poster at 3:30!

Literature:

[1] Kanoh, *Absolute Value Calculating Circuit Having a Single Adder*, US Patent US 4,953,115, 1990

[2] Chirila-Rus (Xilinx Inc.), *Determining Sum of Absolute Differences in Parallel*, US Patent US 8,131,788, 2012

[3] Perri, Zicari & Corsonello, *Efficient Absolute Difference Circuits in Virtex-5 FPGAs*, MELECON 2010